

FIG. 1

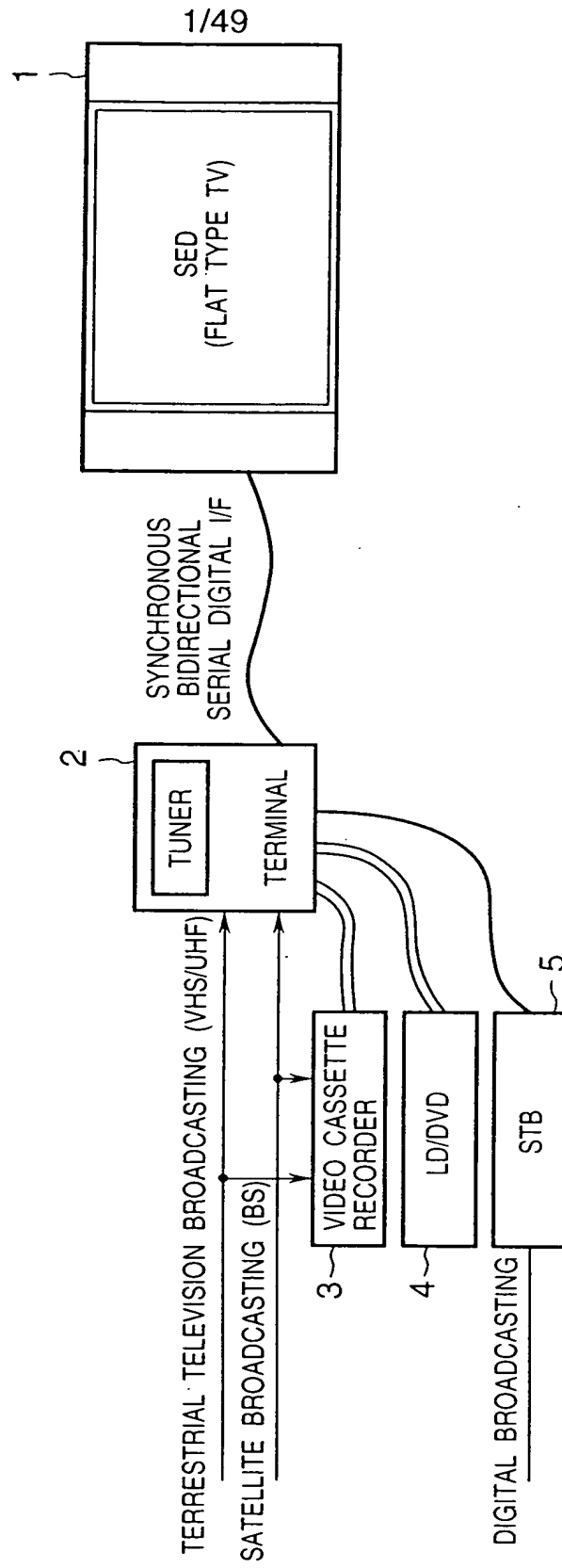


FIG. 2

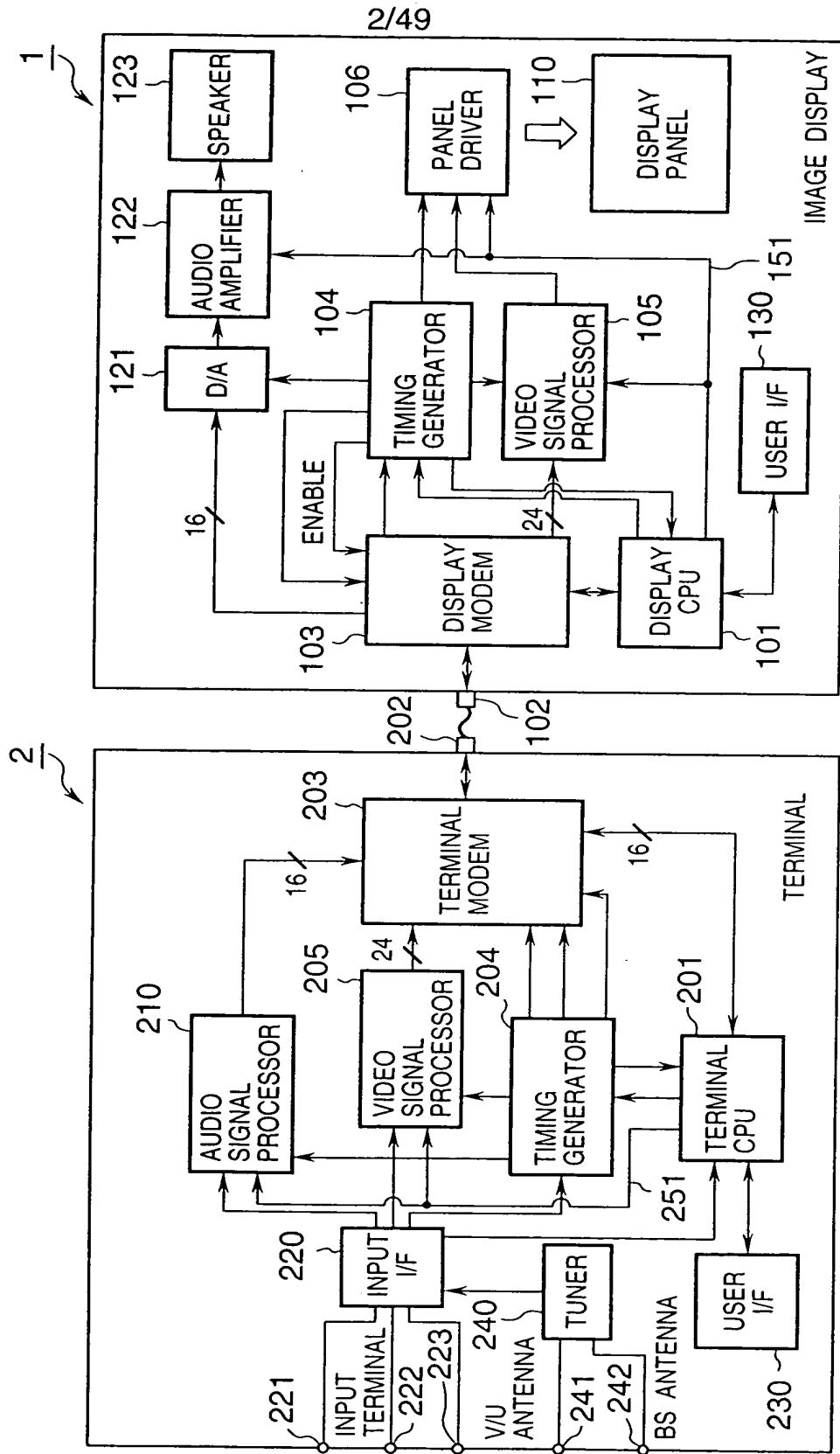


FIG. 3

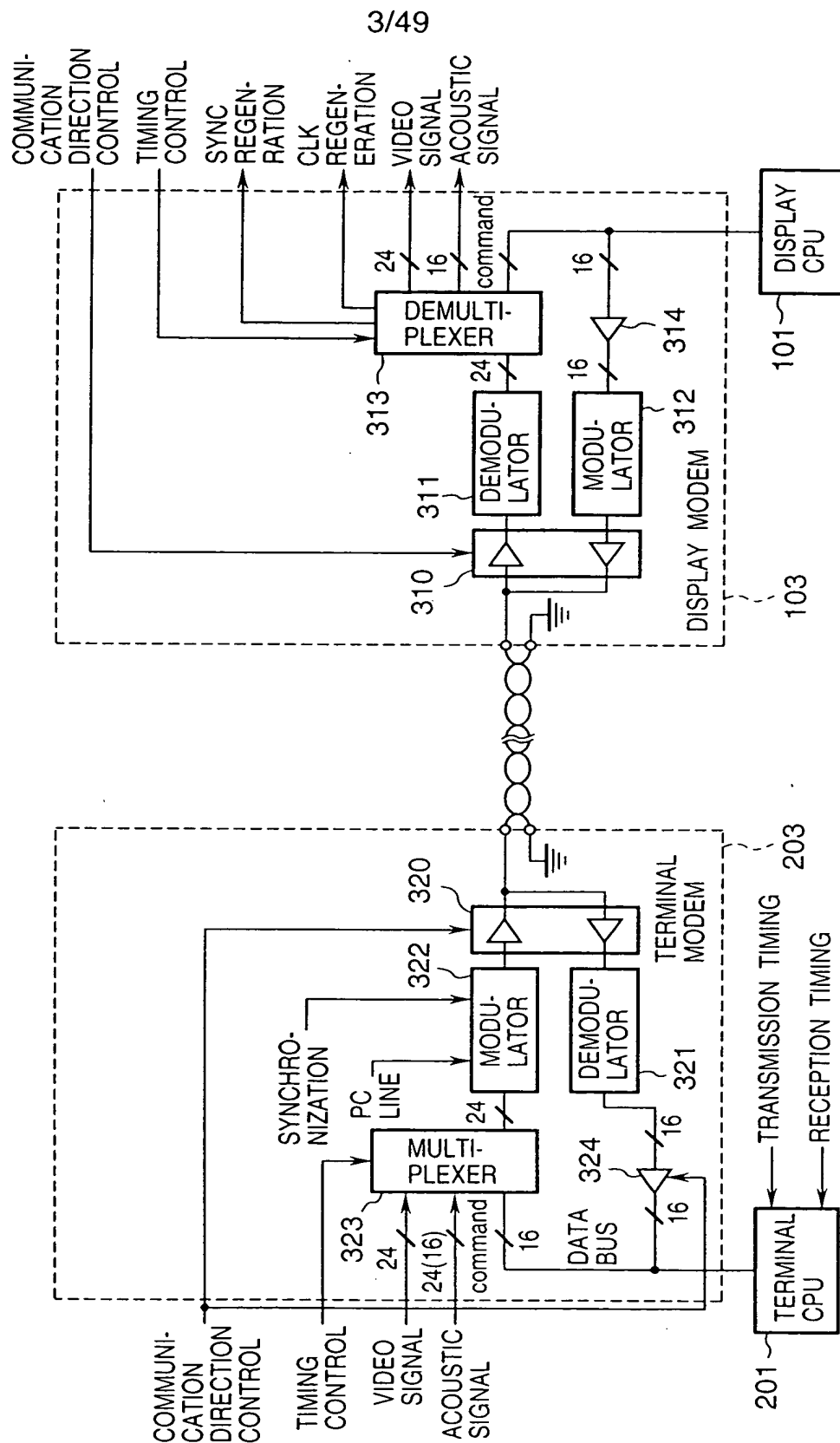


FIG. 4

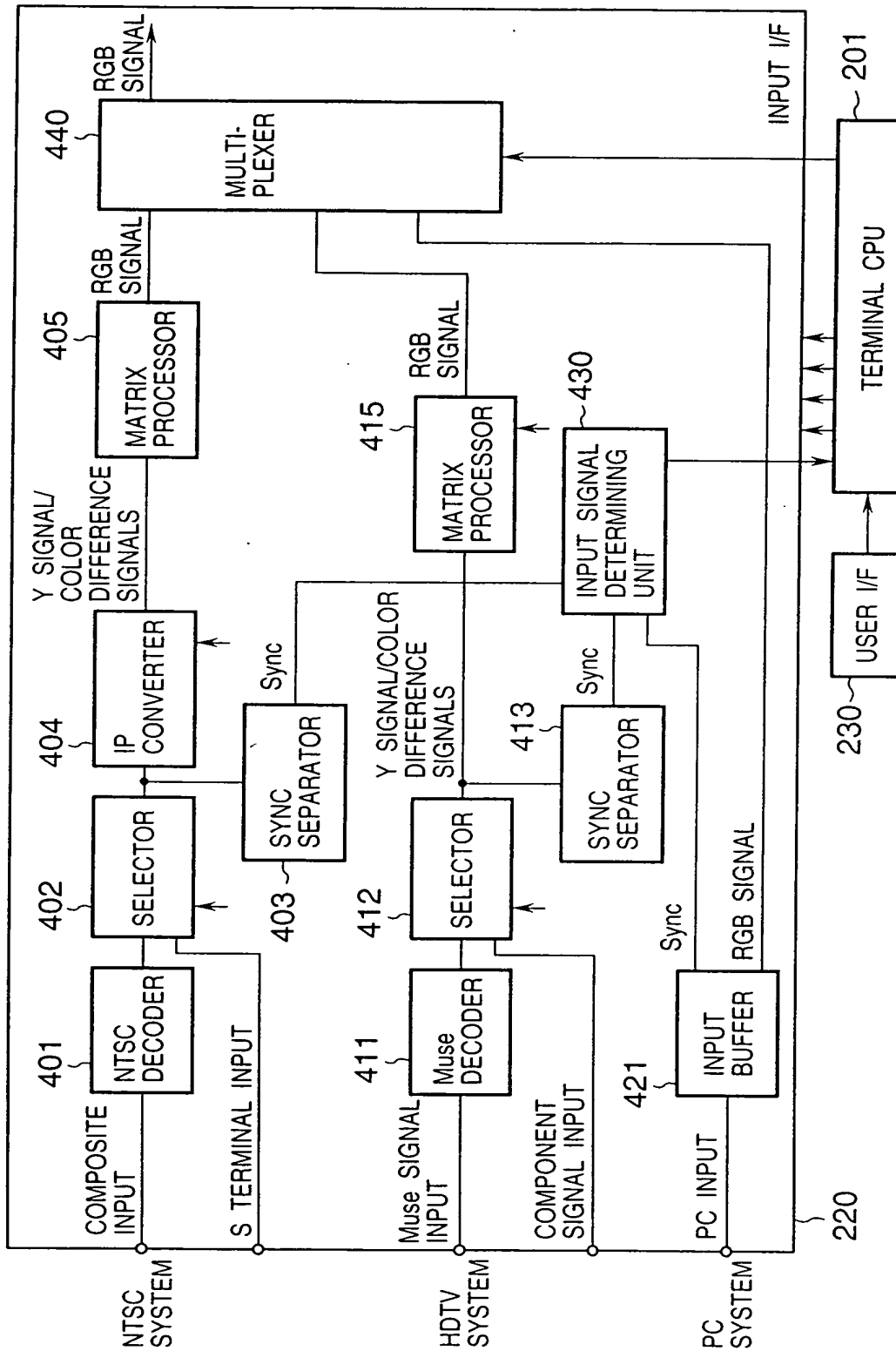


FIG. 5A

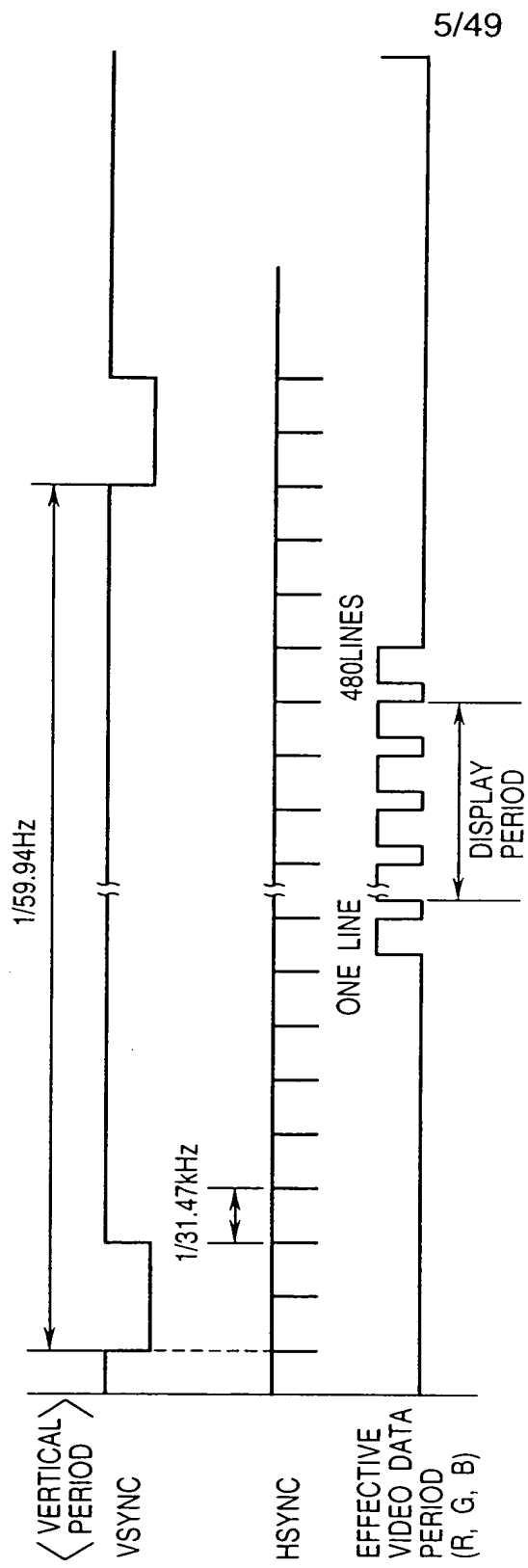


FIG. 5B

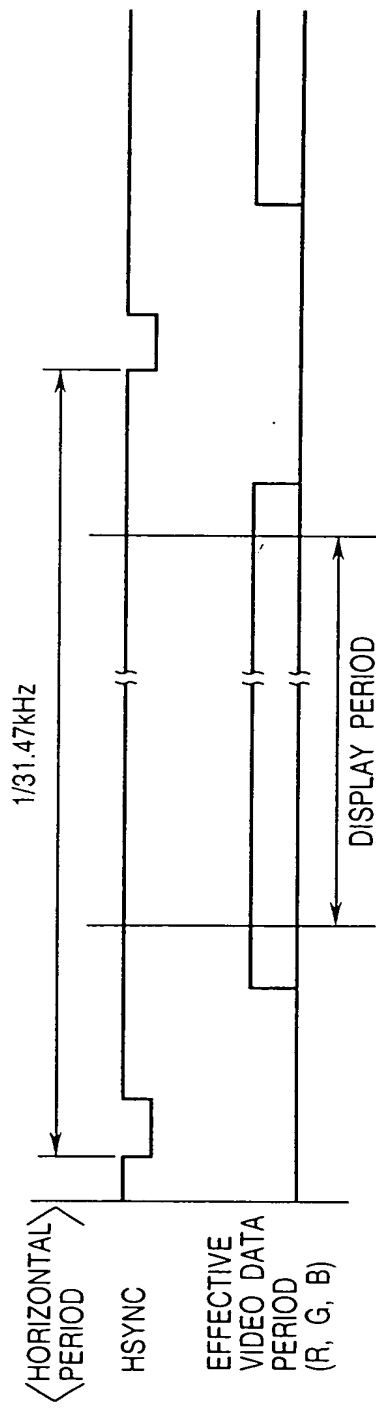
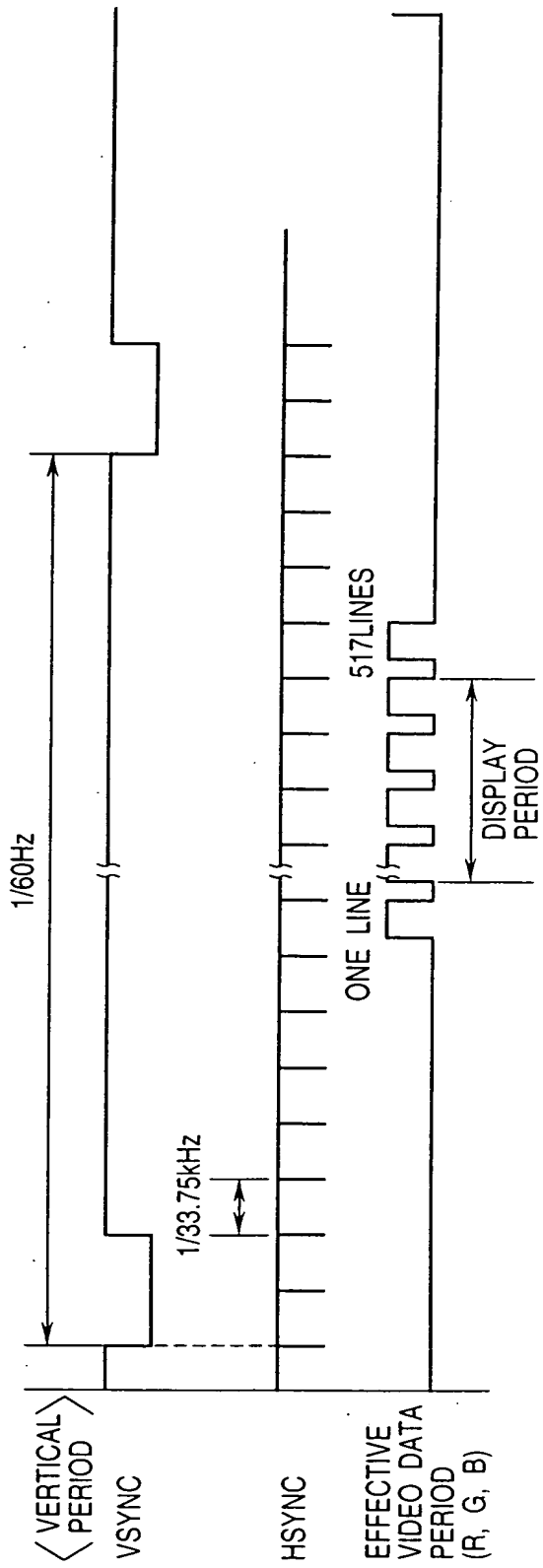


FIG. 6A



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FIG. 6B

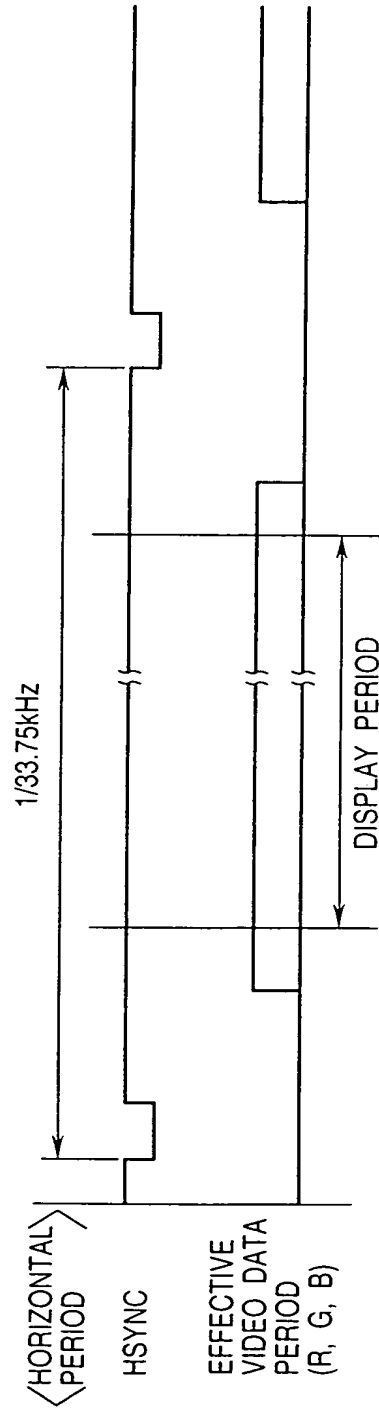


FIG. 7

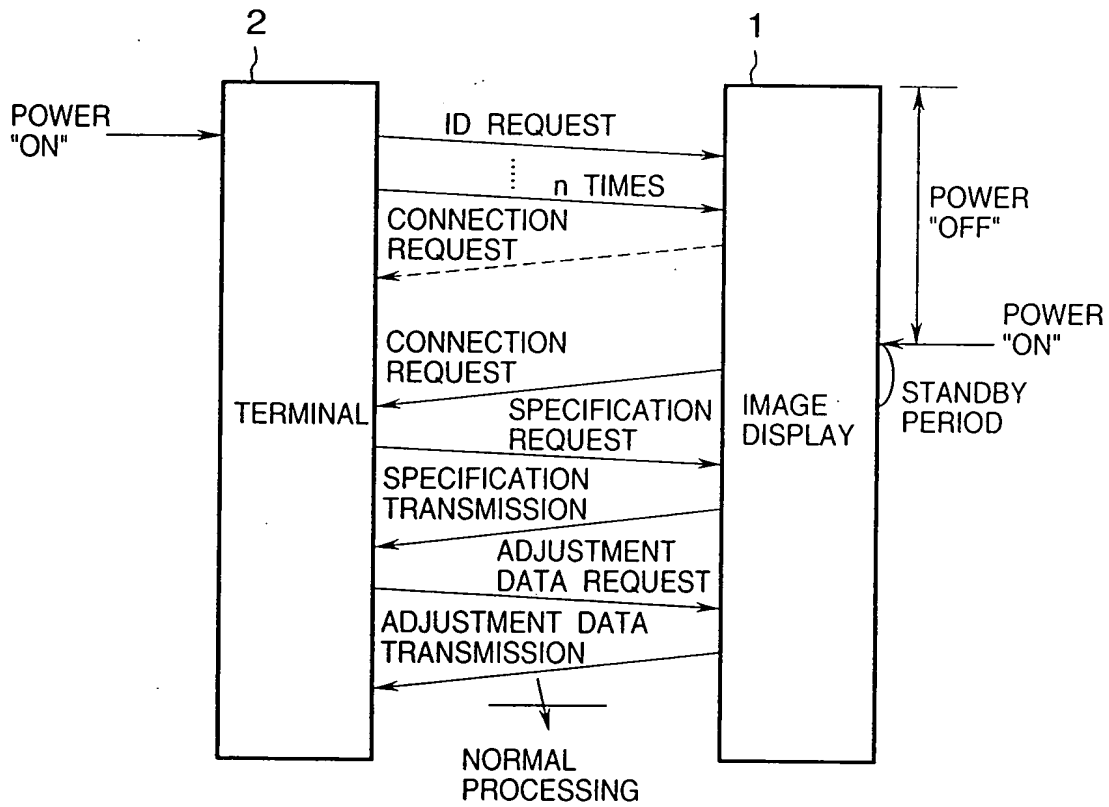


FIG. 8

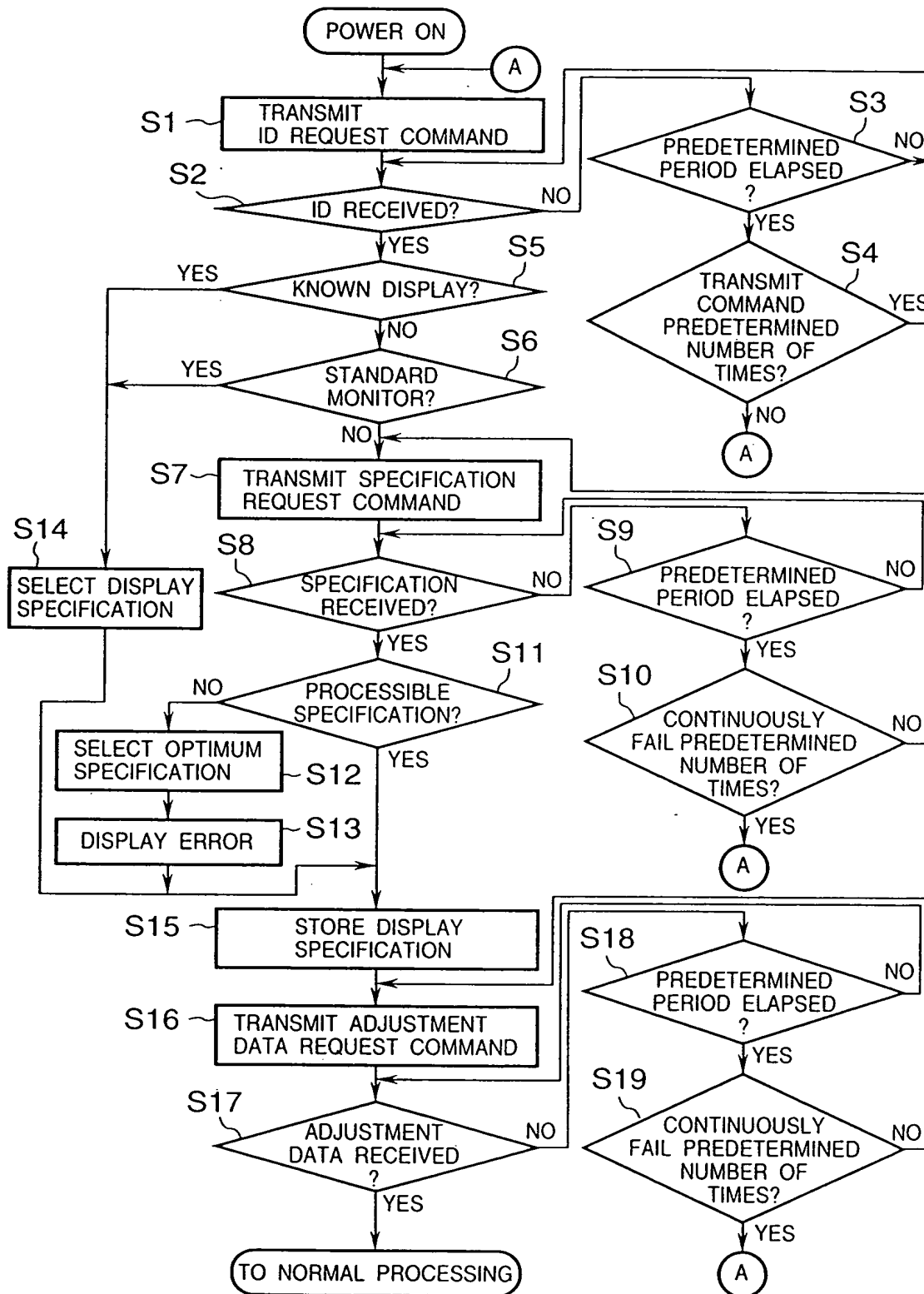


FIG. 9

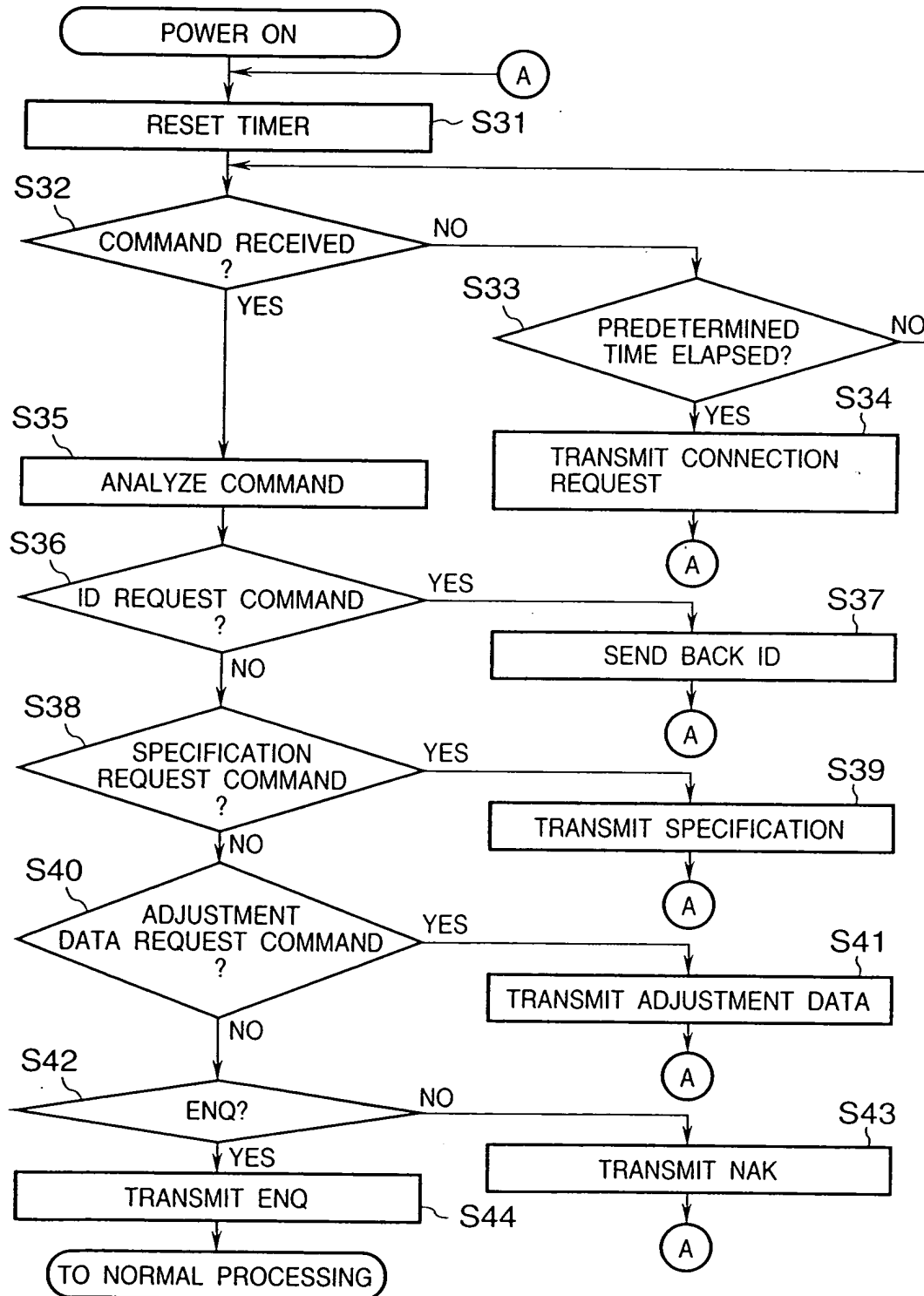


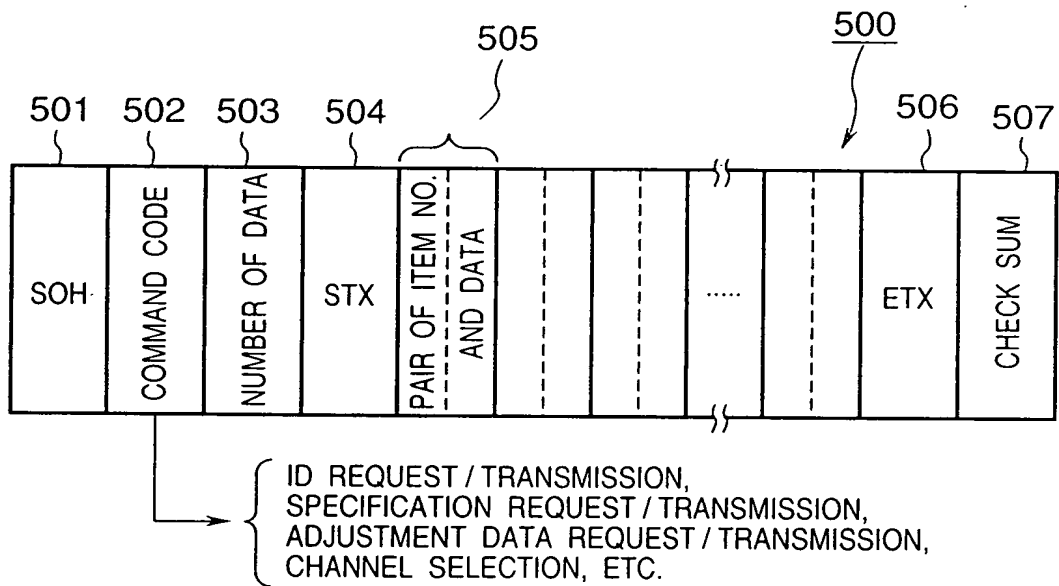
FIG. 10

FIG. 11

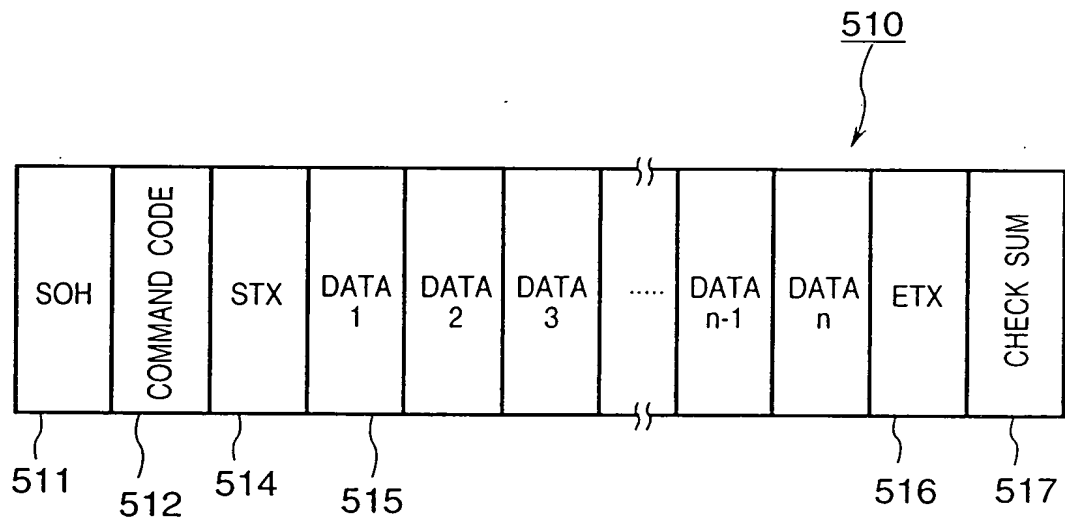


FIG. 12

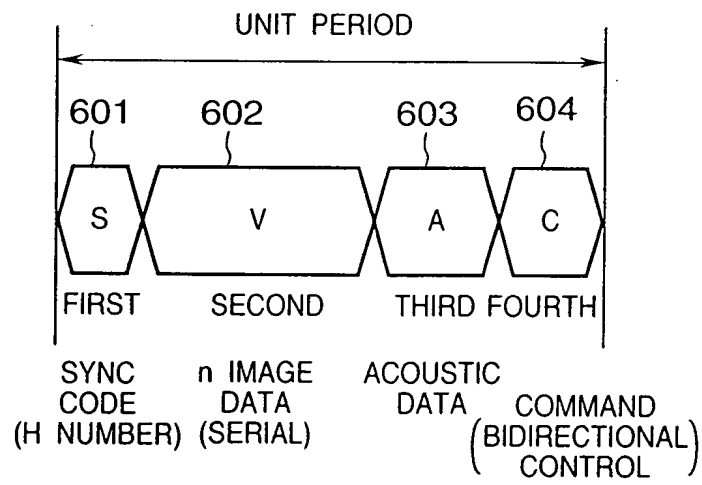


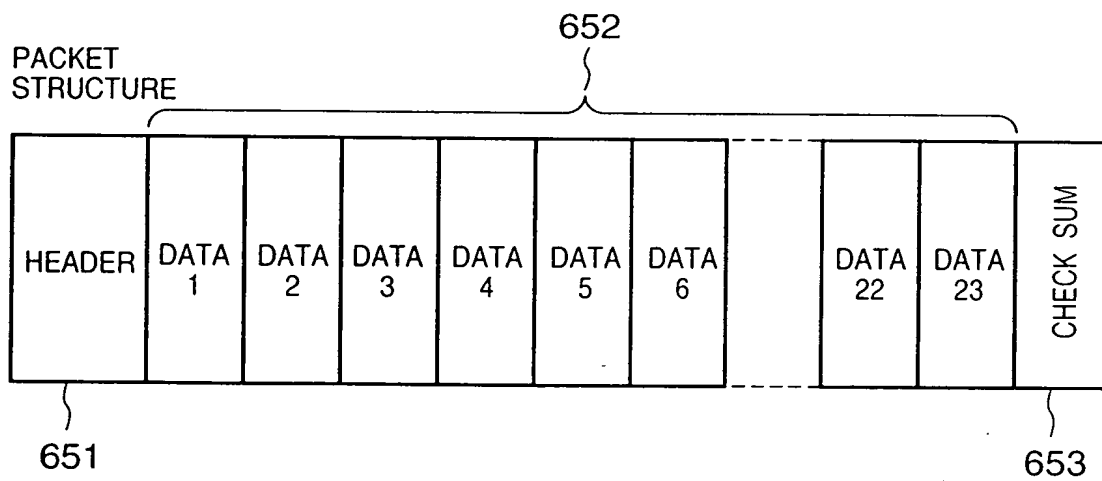
FIG. 13

FIG. 14A

DISPLAY → TERMINAL

HEADER DATA 1	
2	DISPLAY TYPE 1
3	DISPLAY TYPE 2
4	DISPLAY TYPE 3
5	COMMAND 1 (ADJUSTMENT MODE)
6	COMMAND 2 (ADJUSTMENT RIGHT)
7	CONTRAST
8	COLOR TEMPERATURE 1 (G_LEVEL)
9	COLOR TEMPERATURE 2 (B_LEVEL)
10	COLOR TEMPERATURE 3 (R_LEVEL)
11	BRIGHTNESS
12	G_Black LEVEL
13	B_Black LEVEL
14	R_Black LEVEL
15	GAMMA / G_GAMMA
16	B_GAMMA / R_GAMMA
17	DISPLAY MODE
18	HORIZONTAL / VERTICAL DISPLAY SIZE
19	HORIZONTAL / VERTICAL DISPLAY POSITION
20	VOLUME
21	VOLUME L & R BALANCE
22	DISPLAY AUDIO SPECIFICATION
23	
	CHECK SUM

FIG. 14B

TERMINAL → DISPLAY

DATA 1	
2	RECEPTION SIGNAL TYPE 1
3	RECEPTION SIGNAL TYPE 2
4	RECEPTION SIGNAL TYPE 3
5	COMMAND 1 (ADJUSTMENT MODE)
6	COMMAND 2 (ADJUSTMENT RIGHT)
7	CONTRAST
8	COLOR TEMPERATURE 1 (G_LEVEL)
9	COLOR TEMPERATURE 2 (B_LEVEL)
10	COLOR TEMPERATURE 3 (R_LEVEL)
11	BRIGHTNESS
12	G_Black LEVEL
13	B_Black LEVEL
14	R_Black LEVEL
15	GAMMA / G_GAMMA
16	B_GAMMA / R_GAMMA
17	DISPLAY MODE
18	HORIZONTAL / VERTICAL DISPLAY SIZE
19	HORIZONTAL / VERTICAL DISPLAY POSITION
20	VOLUME
21	VOLUME L & R BALANCE
22	
23	
	CHECK SUM

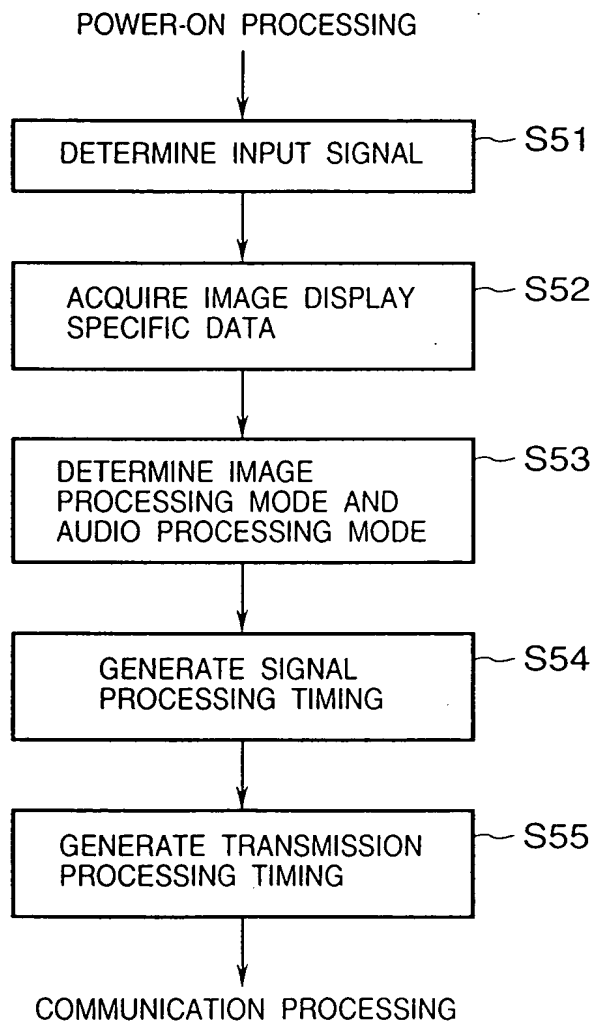
FIG. 15

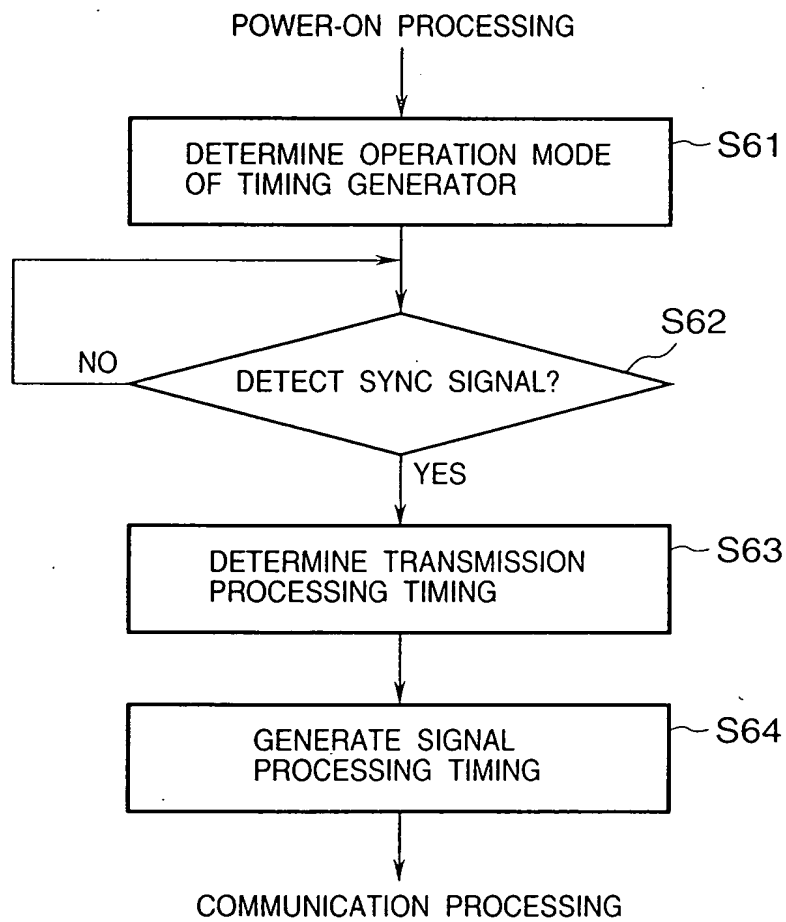
FIG. 16

FIG. 17

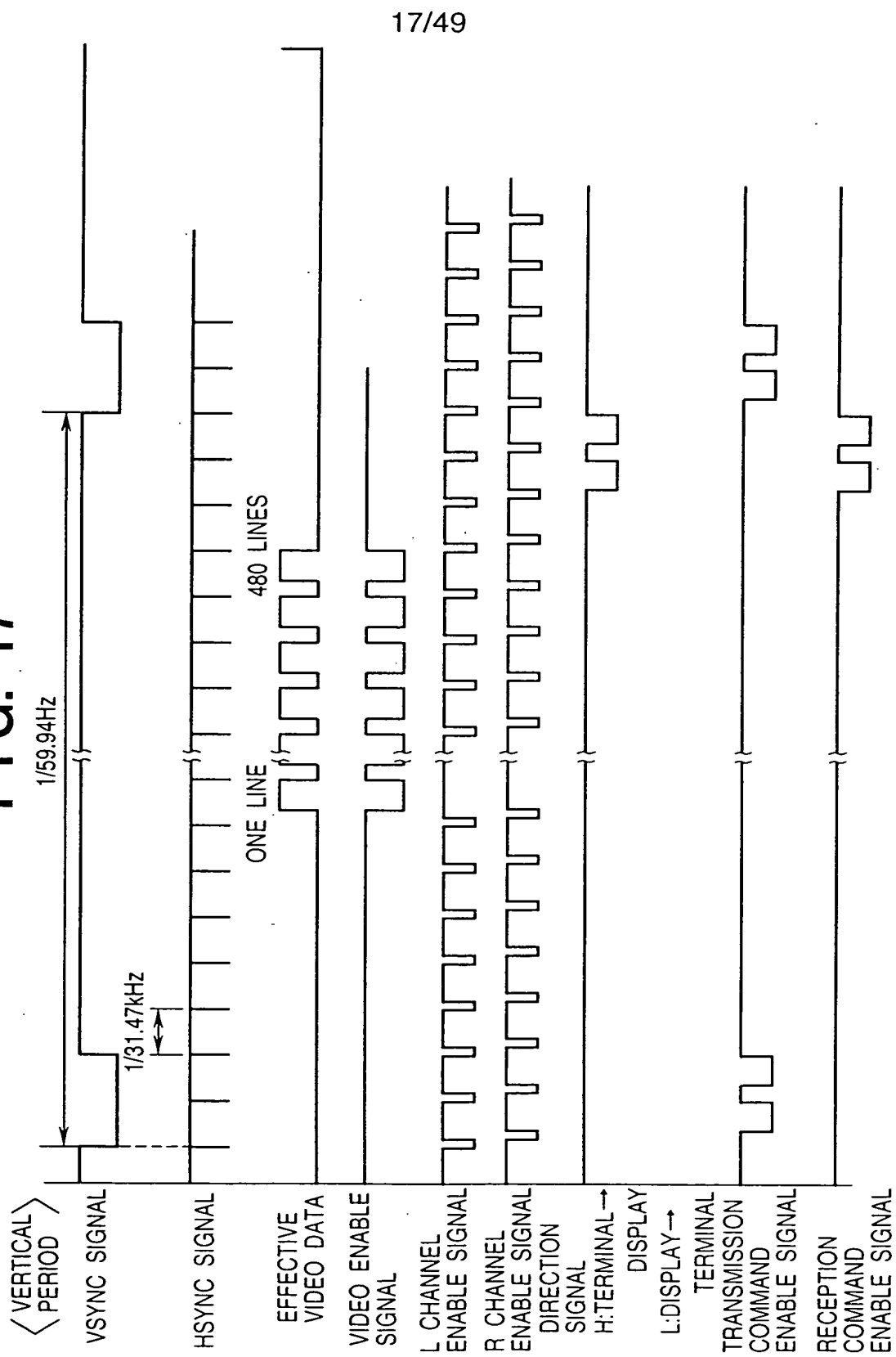


FIG. 18

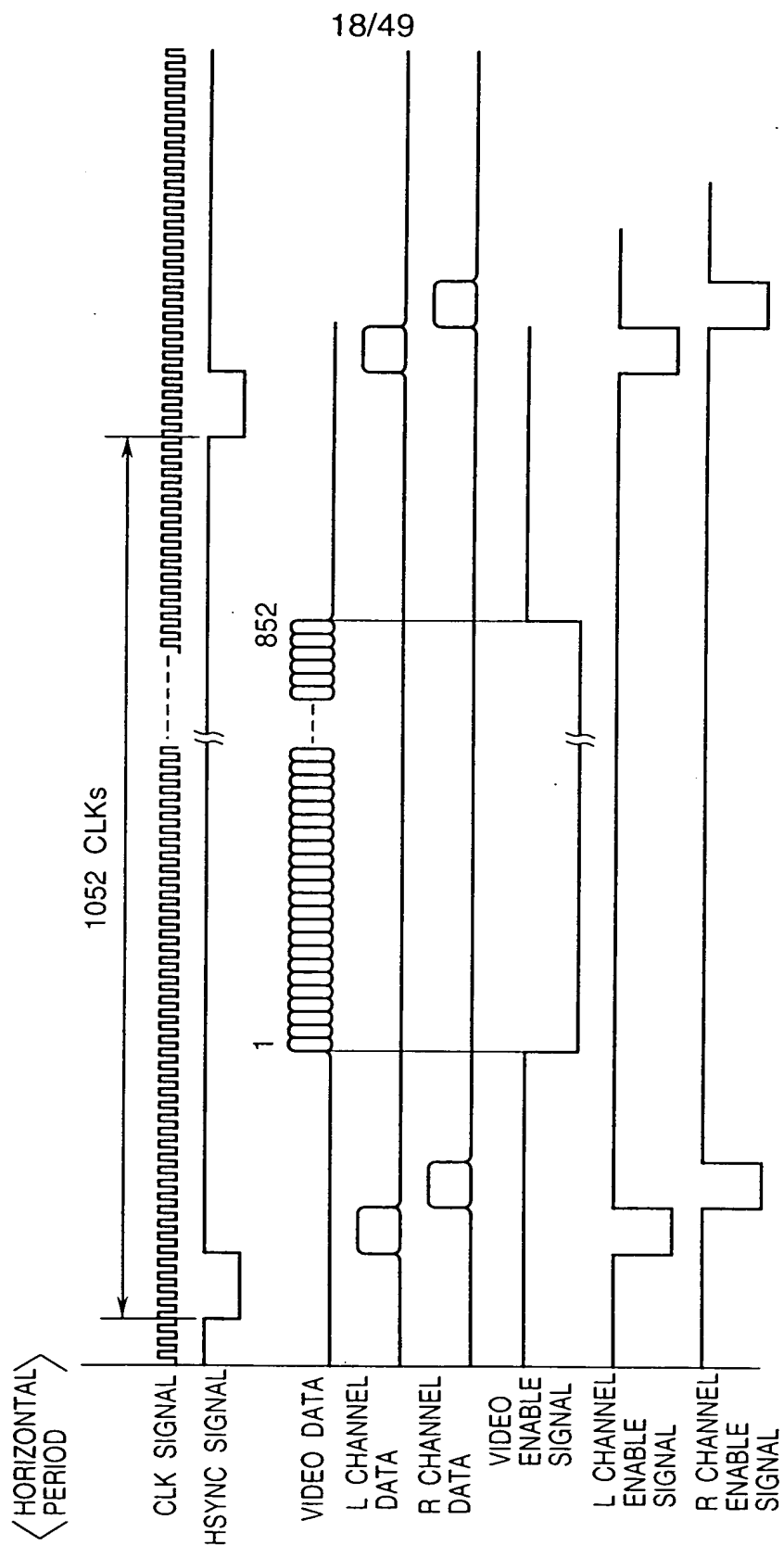


FIG. 19

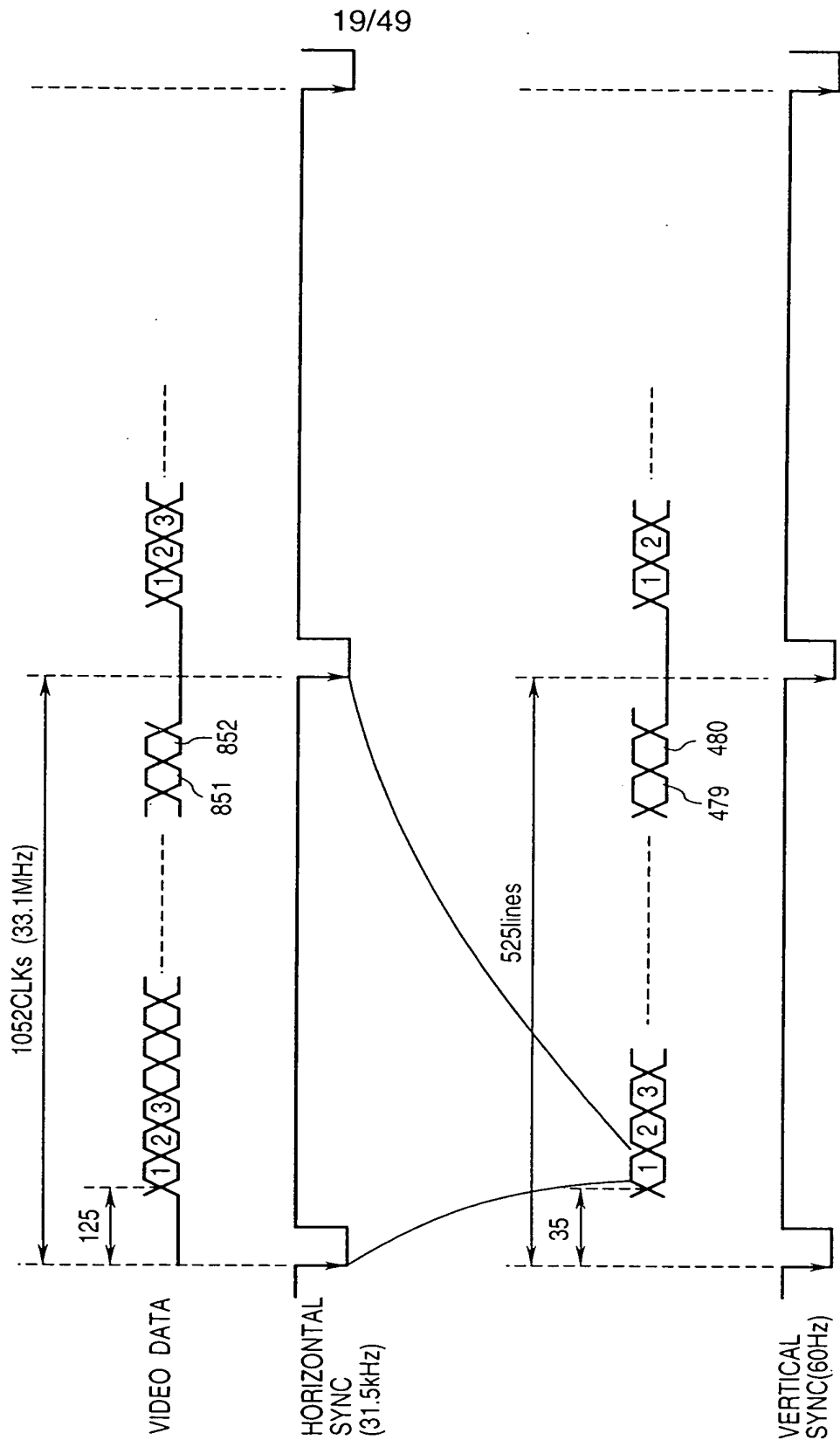


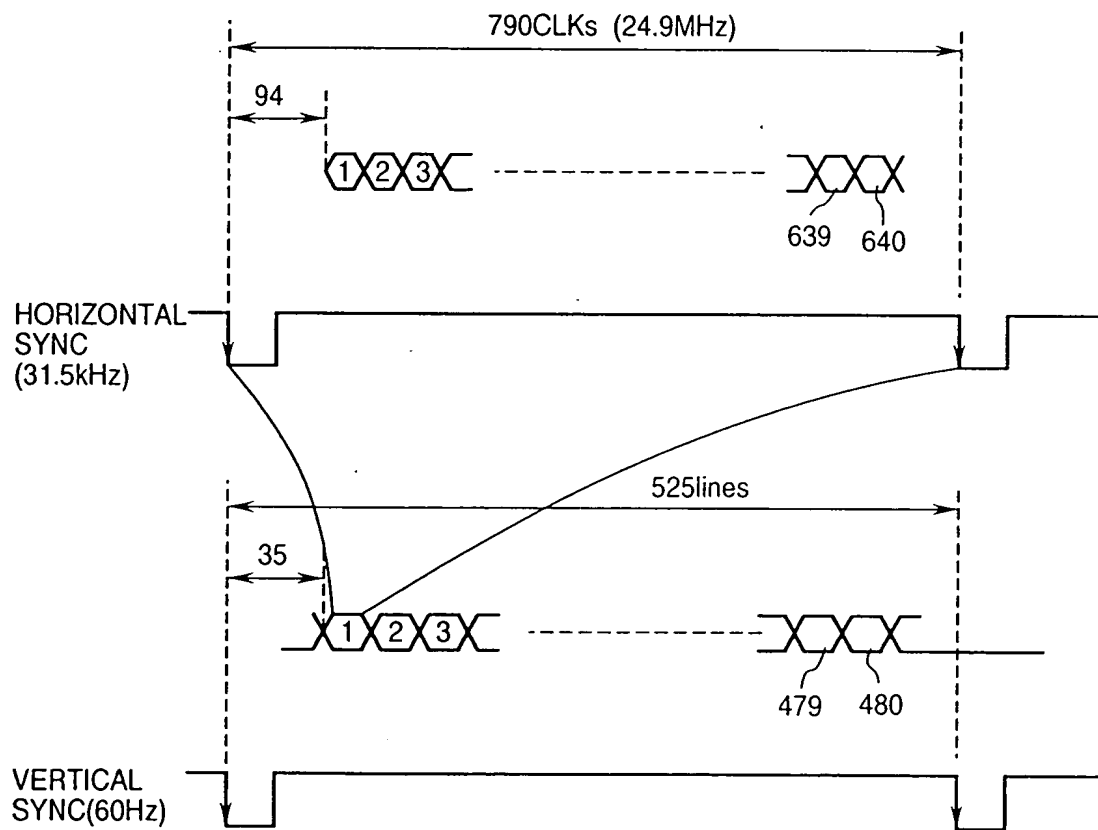
FIG. 20

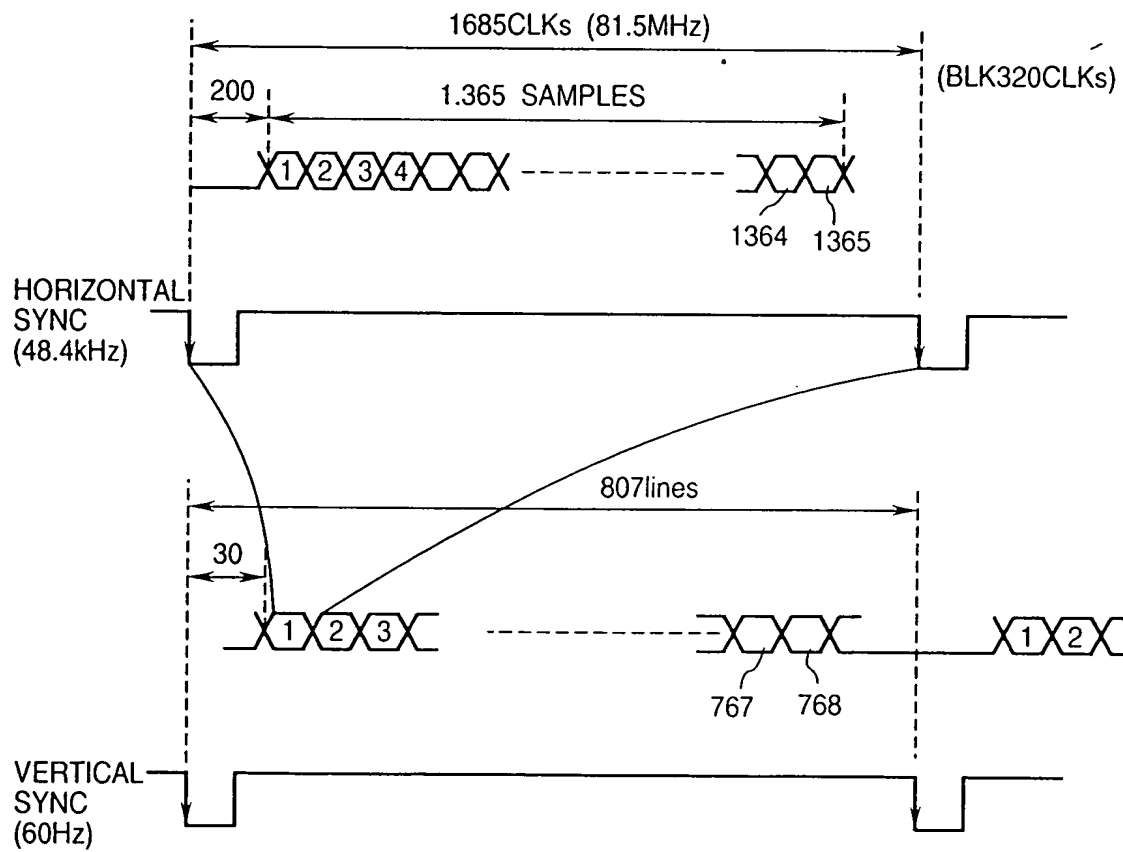
FIG. 21

FIG. 22

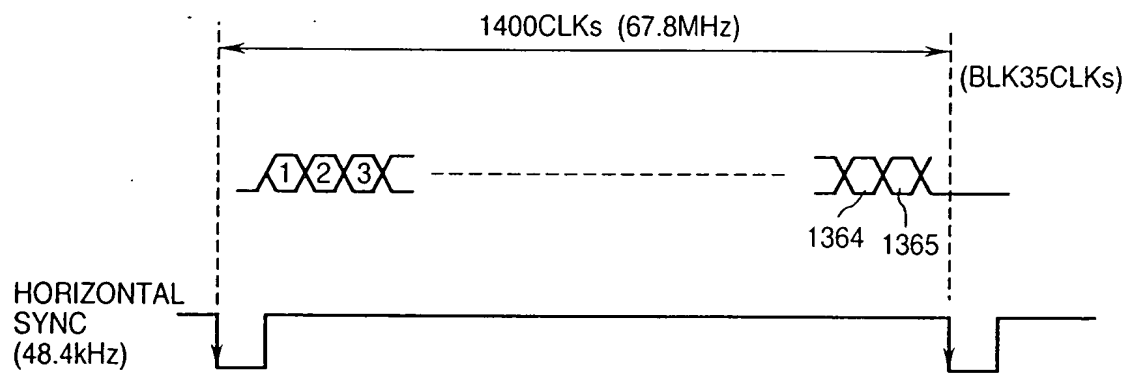


FIG. 23

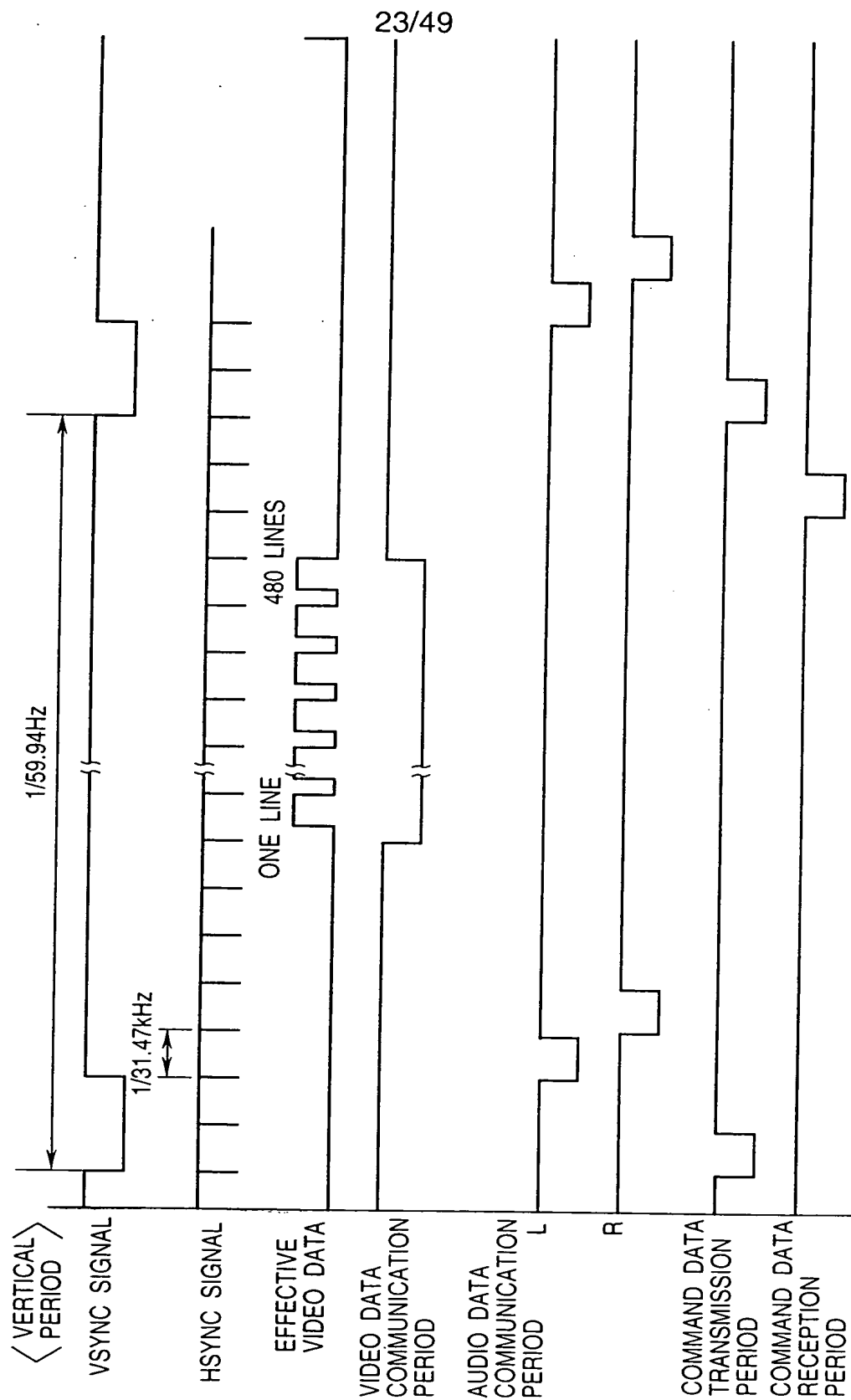


FIG. 24

< HORIZONTAL
PERIOD >

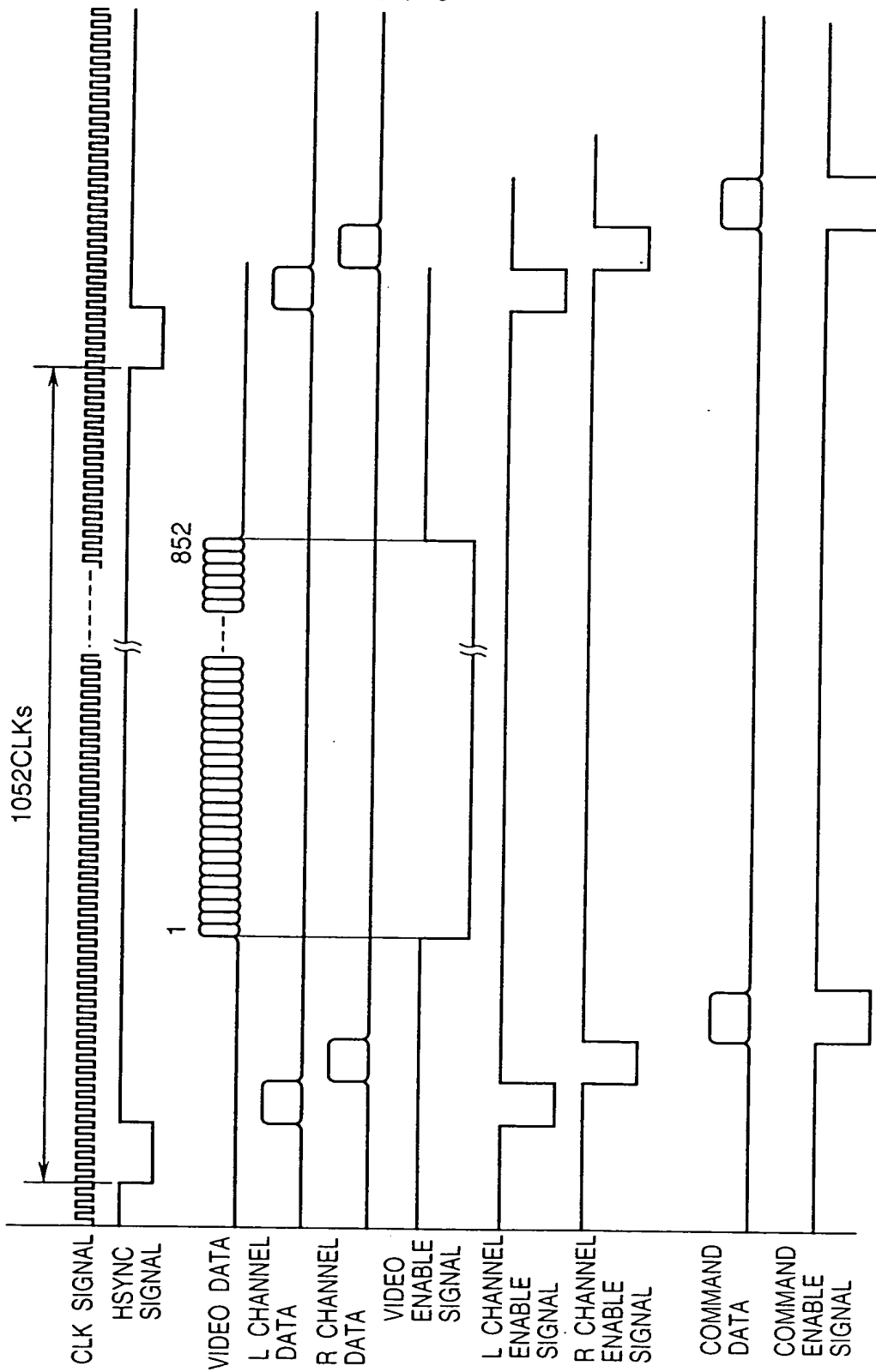


FIG. 25

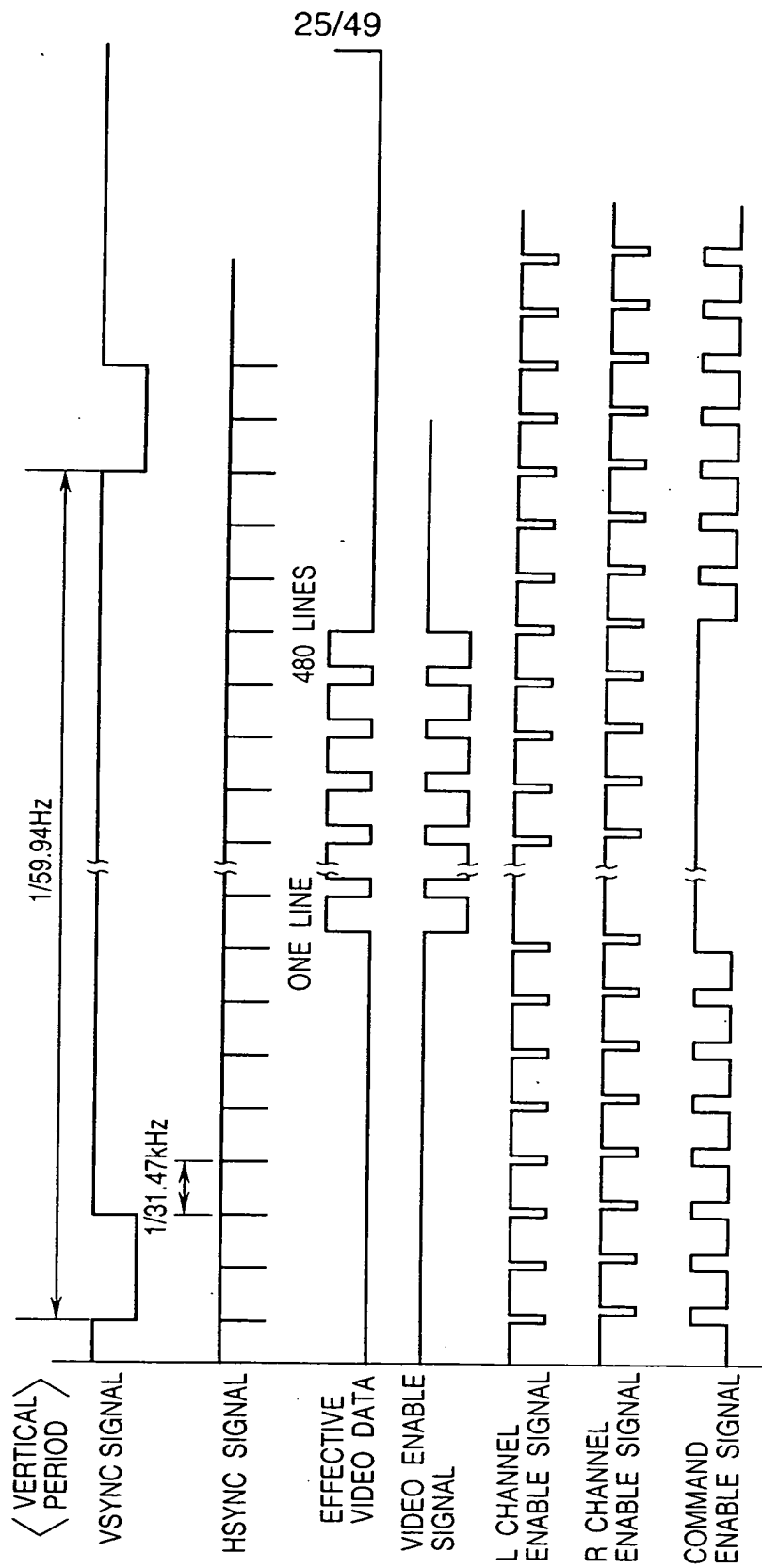


FIG. 26

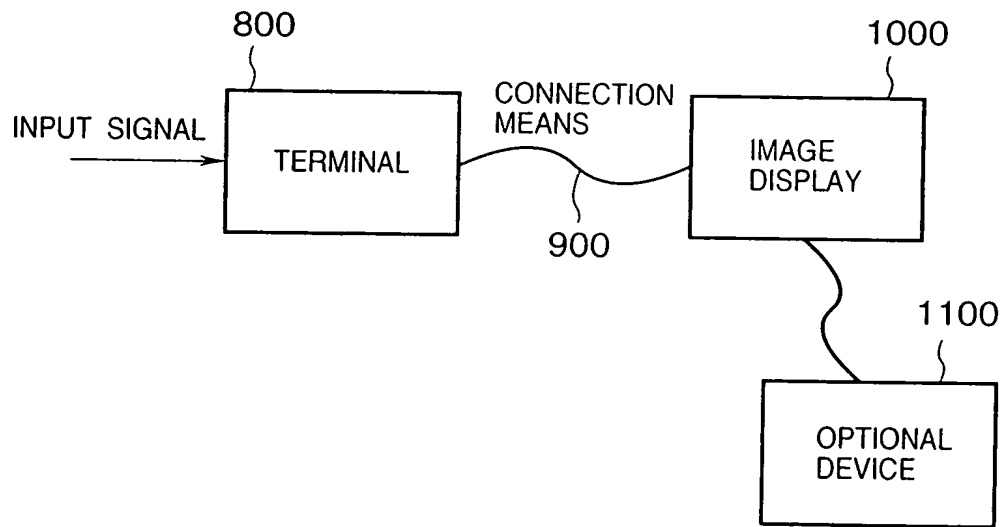


FIG. 27

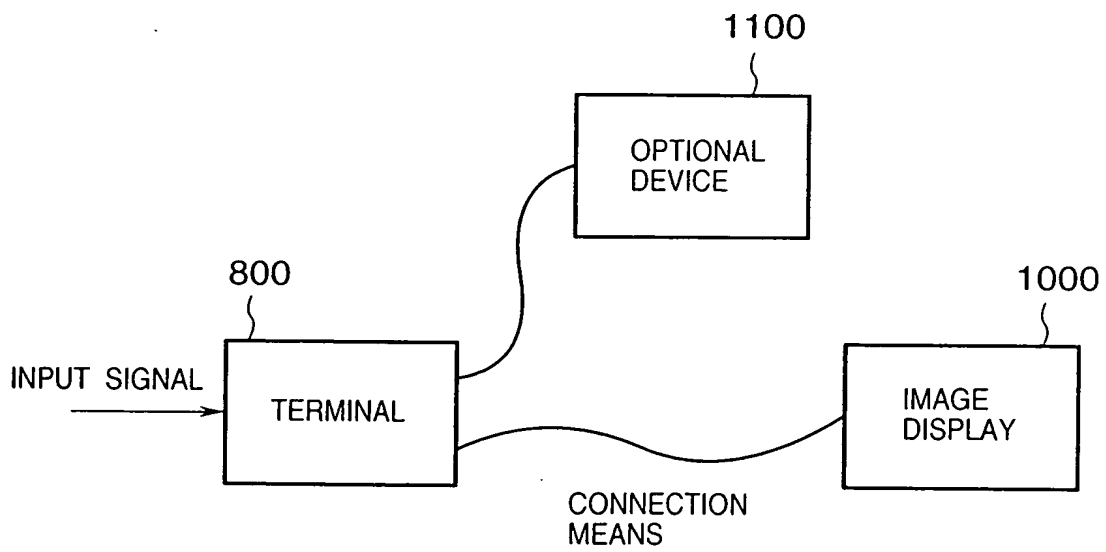


FIG. 28

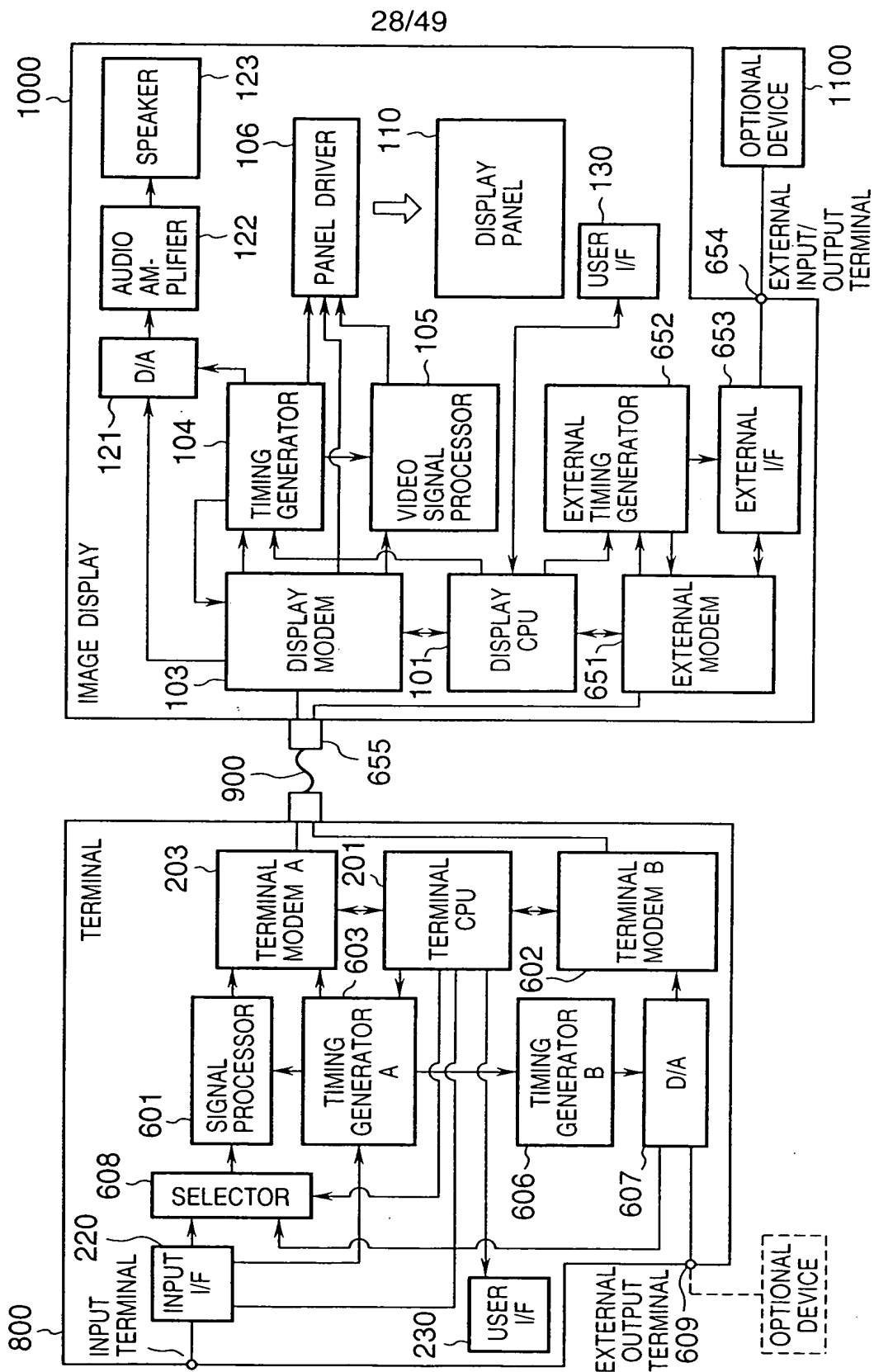


FIG. 29

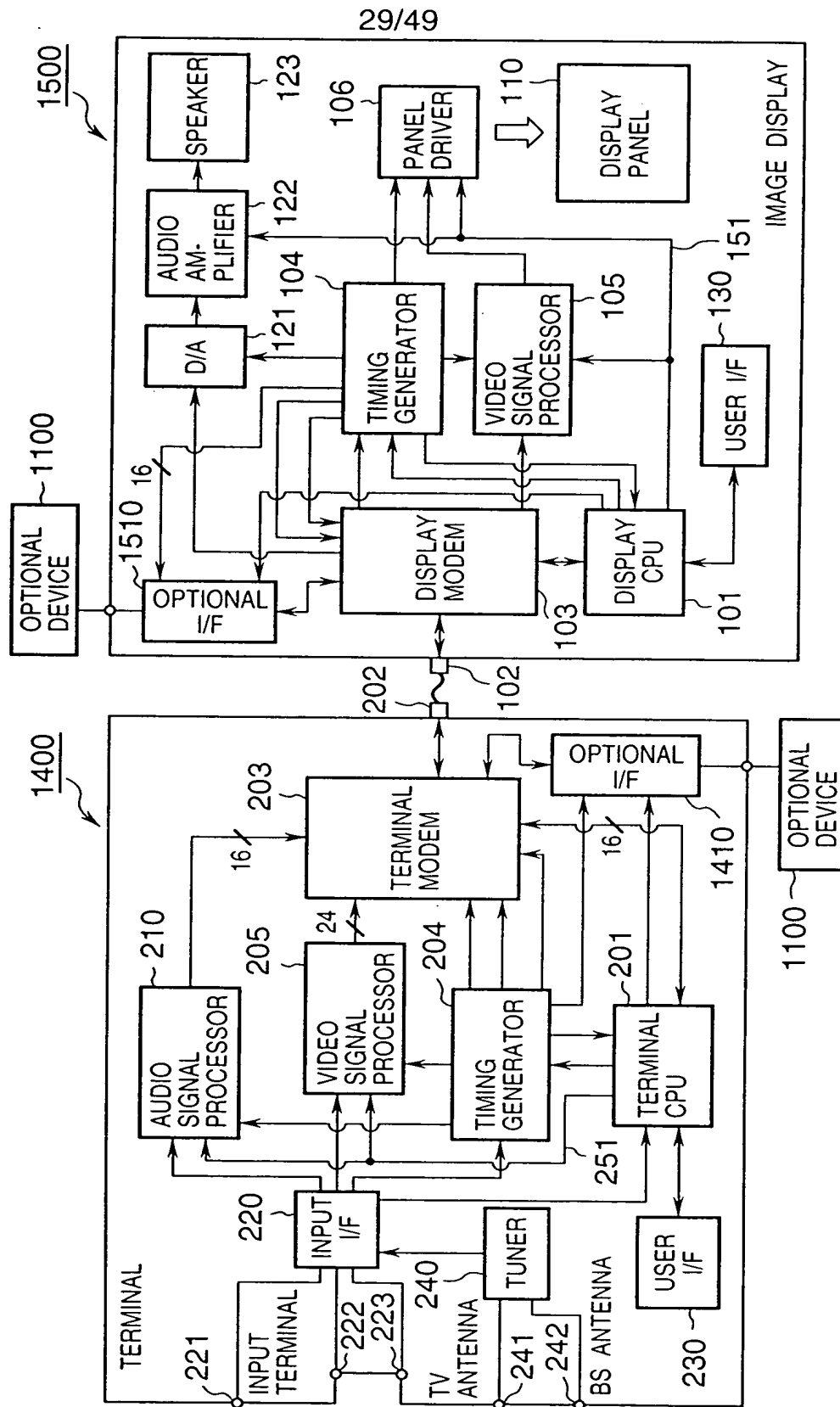


FIG. 30

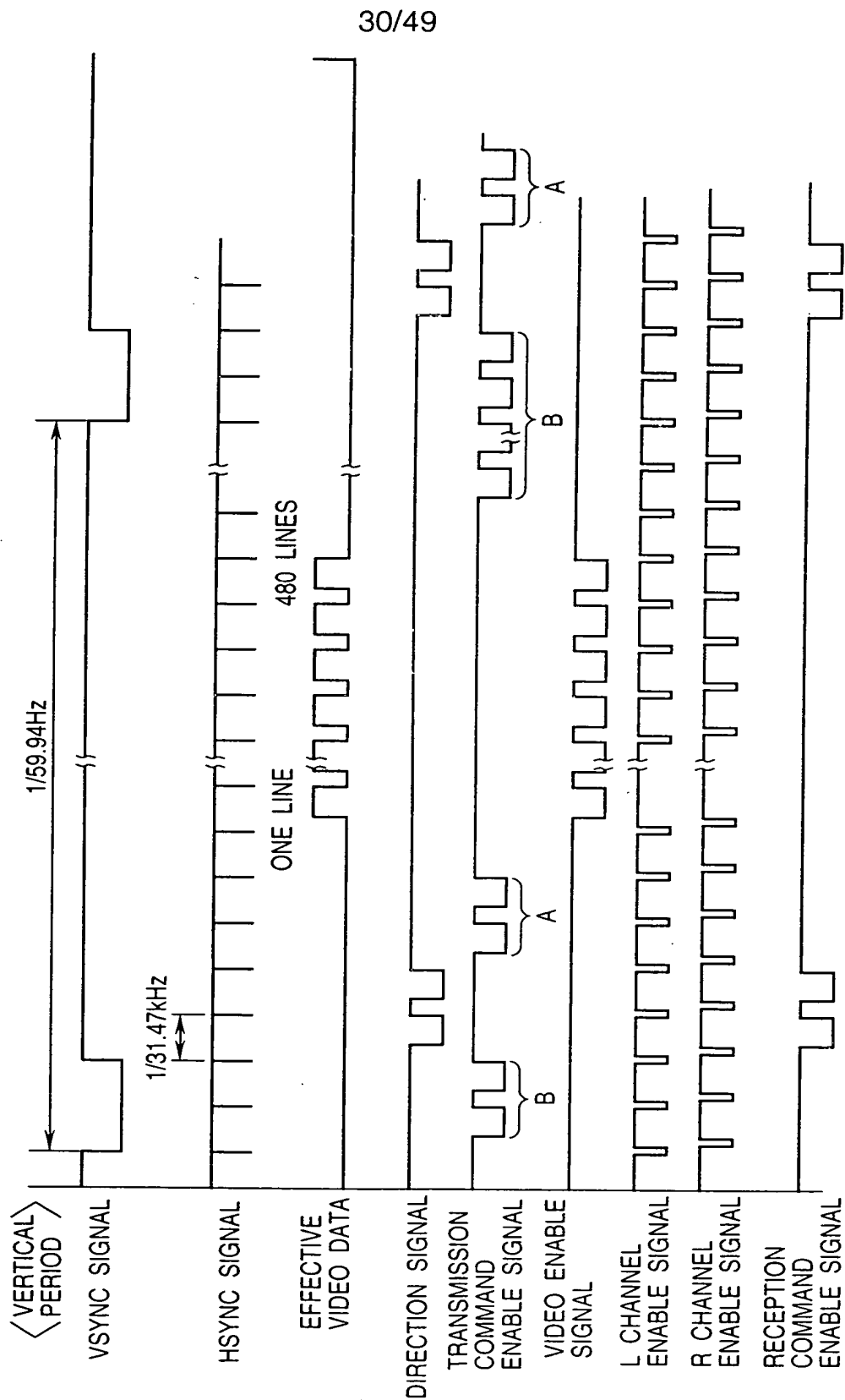


FIG. 31

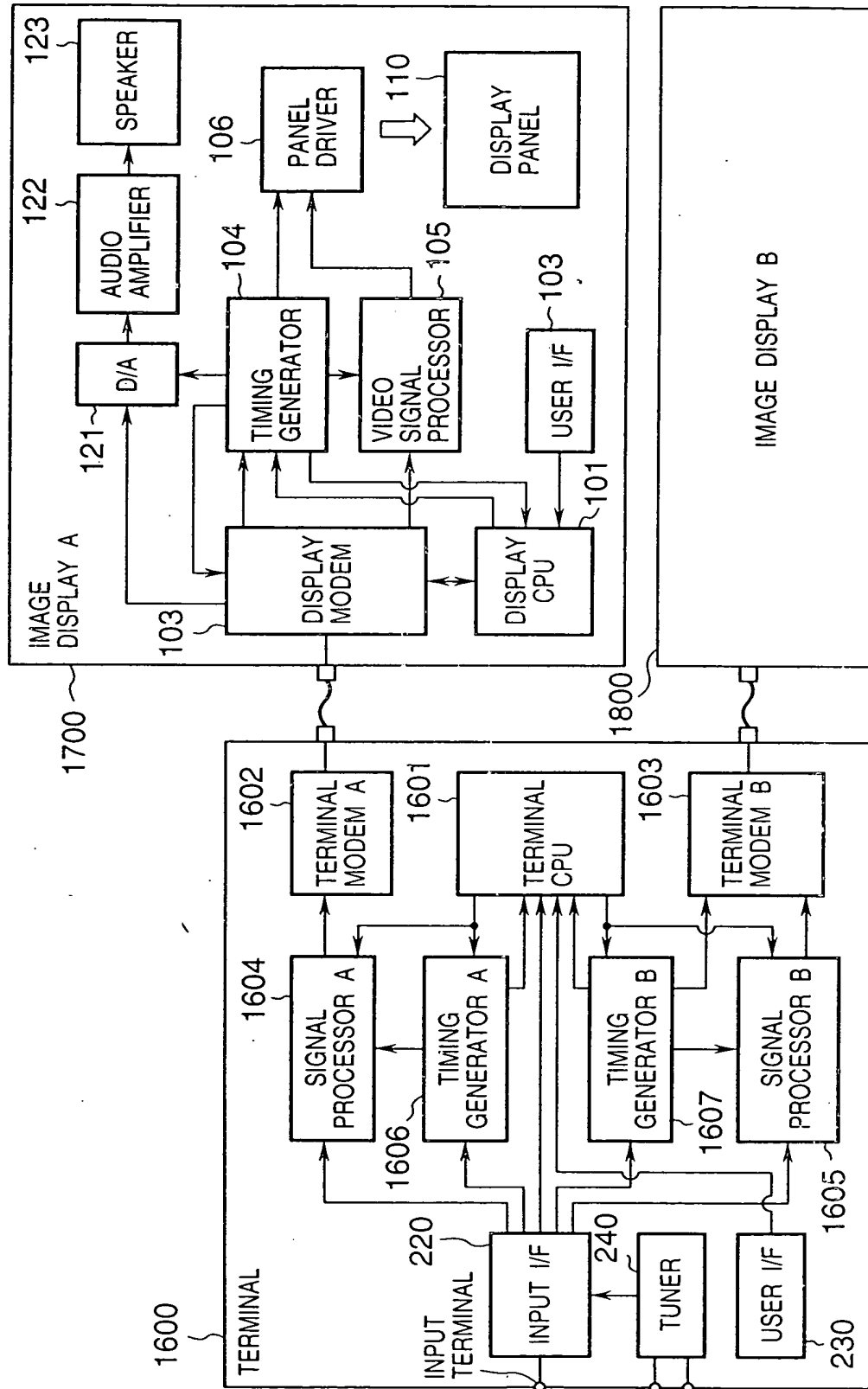


FIG. 32

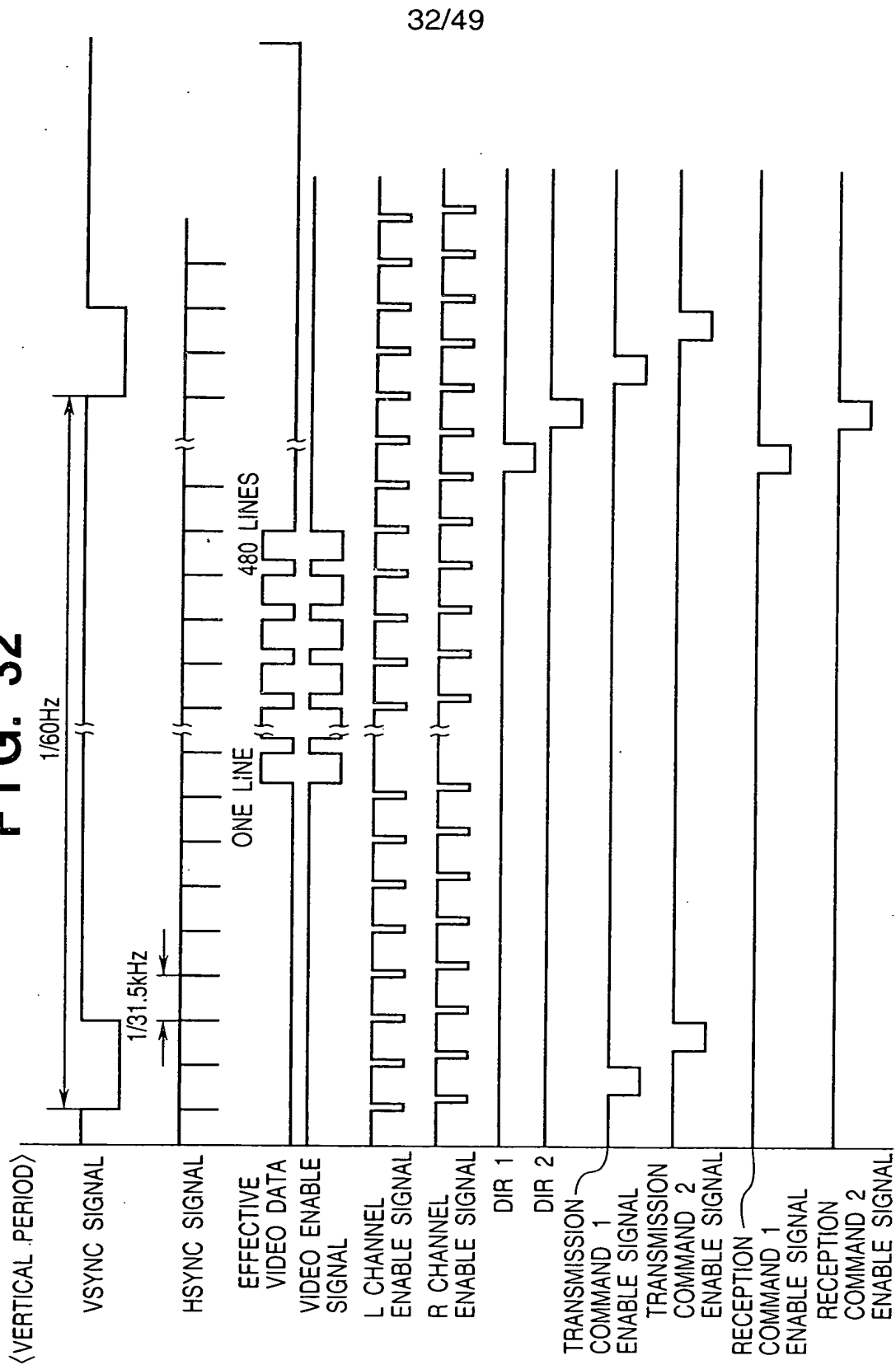


FIG. 33

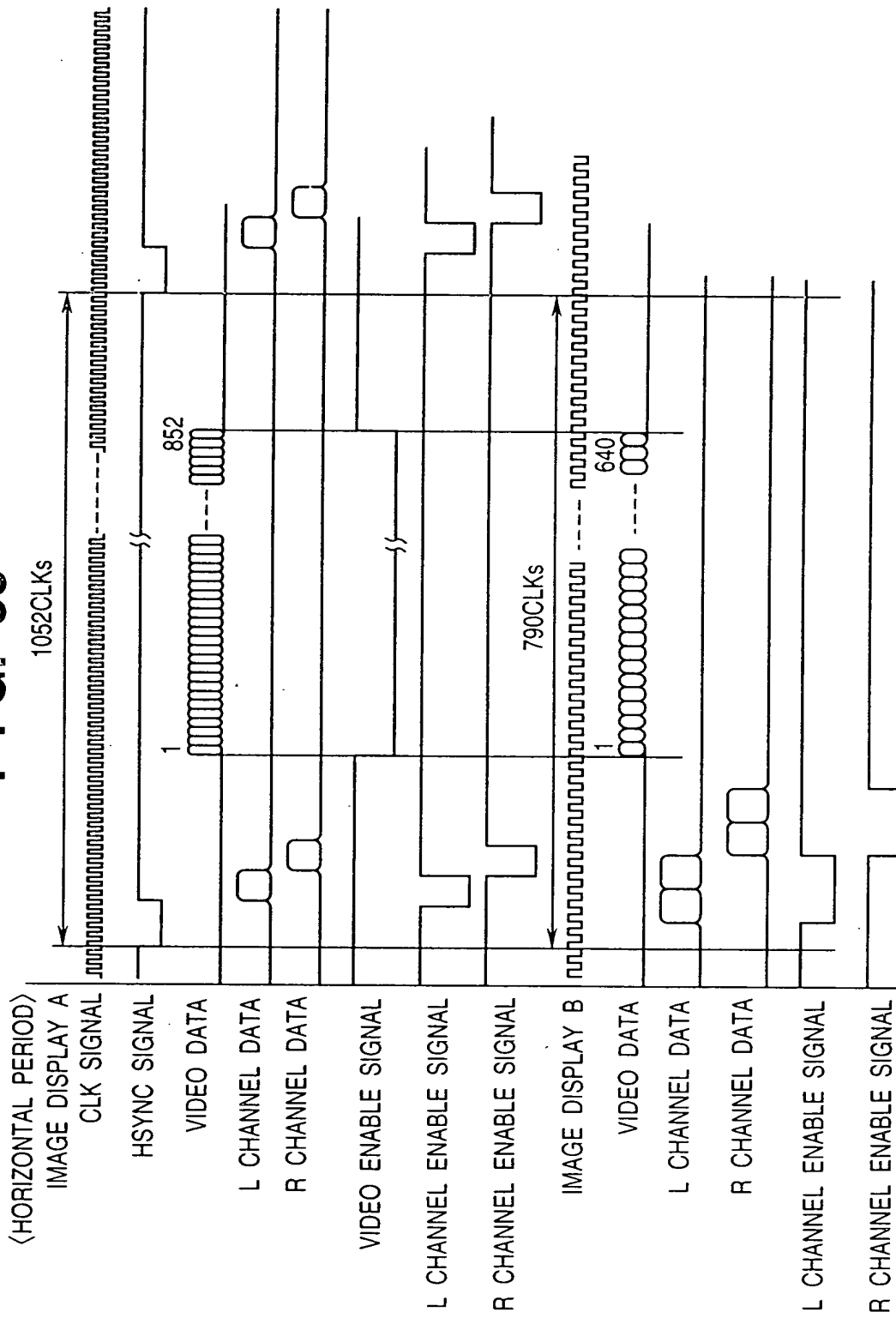


FIG. 34

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The diagram illustrates a video display system architecture. At the top, a **TERMINAL** (200) is shown, which includes an **INPUT TERMINAL** (220), an **INPUT I/F** (240), a **TUNER** (240), a **TIMING GENERATOR** (204), a **SIGNAL PROCESSOR** (250), a **TERMINAL CPU** (201), a **TERMINAL MODEM** (203), and a **USER I/F** (230). The terminal is connected to two **IMAGE DISPLAY** units, **A** and **B**. Each display unit contains a **DRIVER** (150), a **DISPLAY MODEM** (103), a **TIMING GENERATOR** (121), a **D/A** converter (121), an **AUDIO AMPLIFIER** (123), a **SPEAKER** (123), a **PANEL DRIVER** (106), a **DISPLAY PANEL** (110), a **VIDEO SIGNAL PROCESSOR** (105), a **DISPLAY CPU** (101), and a **USER I/F** (151 for A, 130 for B). An **OPTIONAL DEVICE** (2100) is connected to the terminal and both displays via a bus (2200). The diagram is labeled **FIG. 34** and **34/49**.

FIG. 35

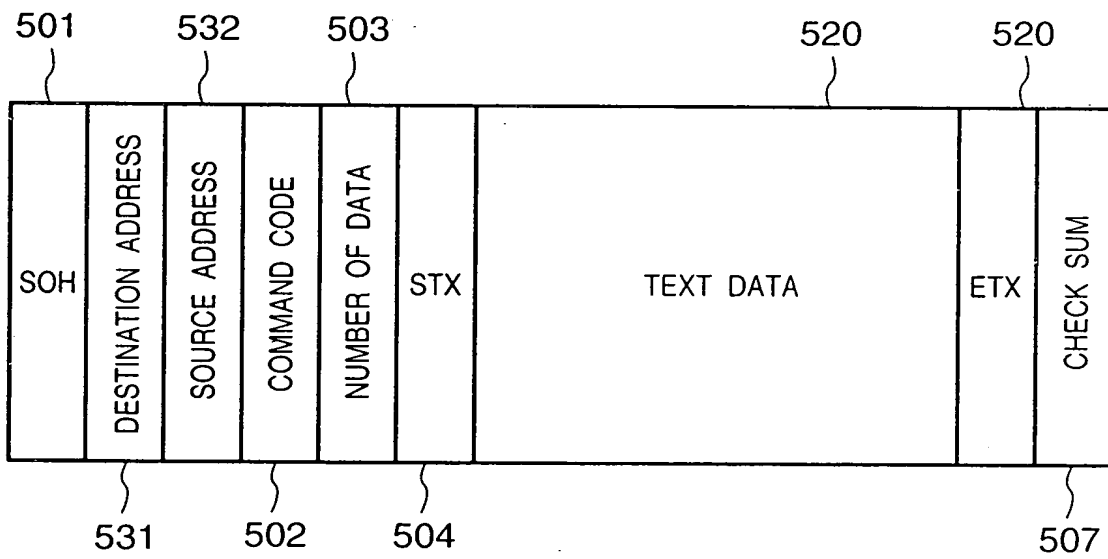


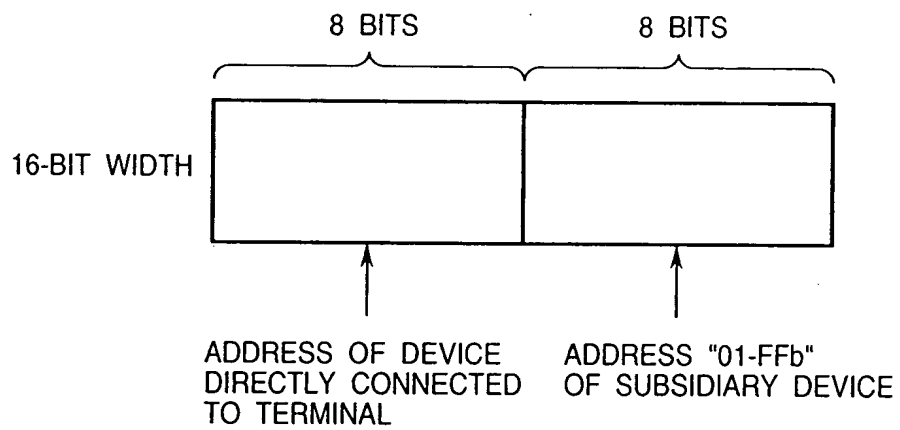
FIG. 36

FIG. 37

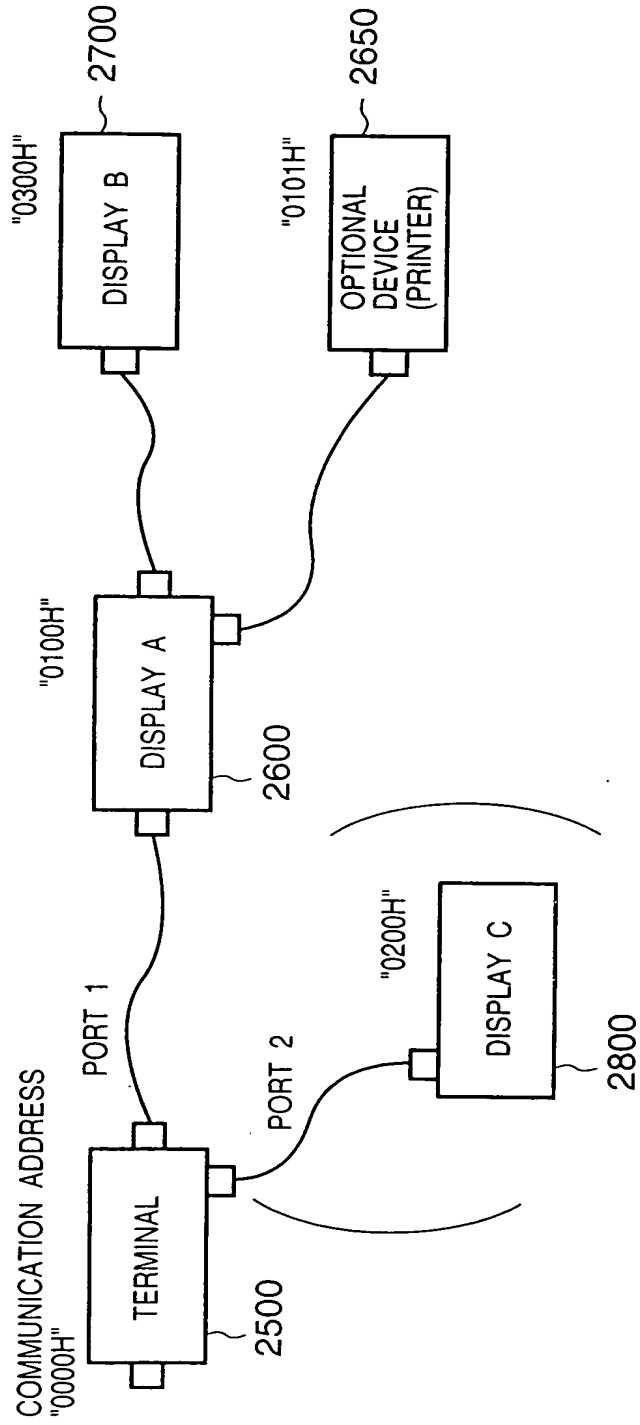


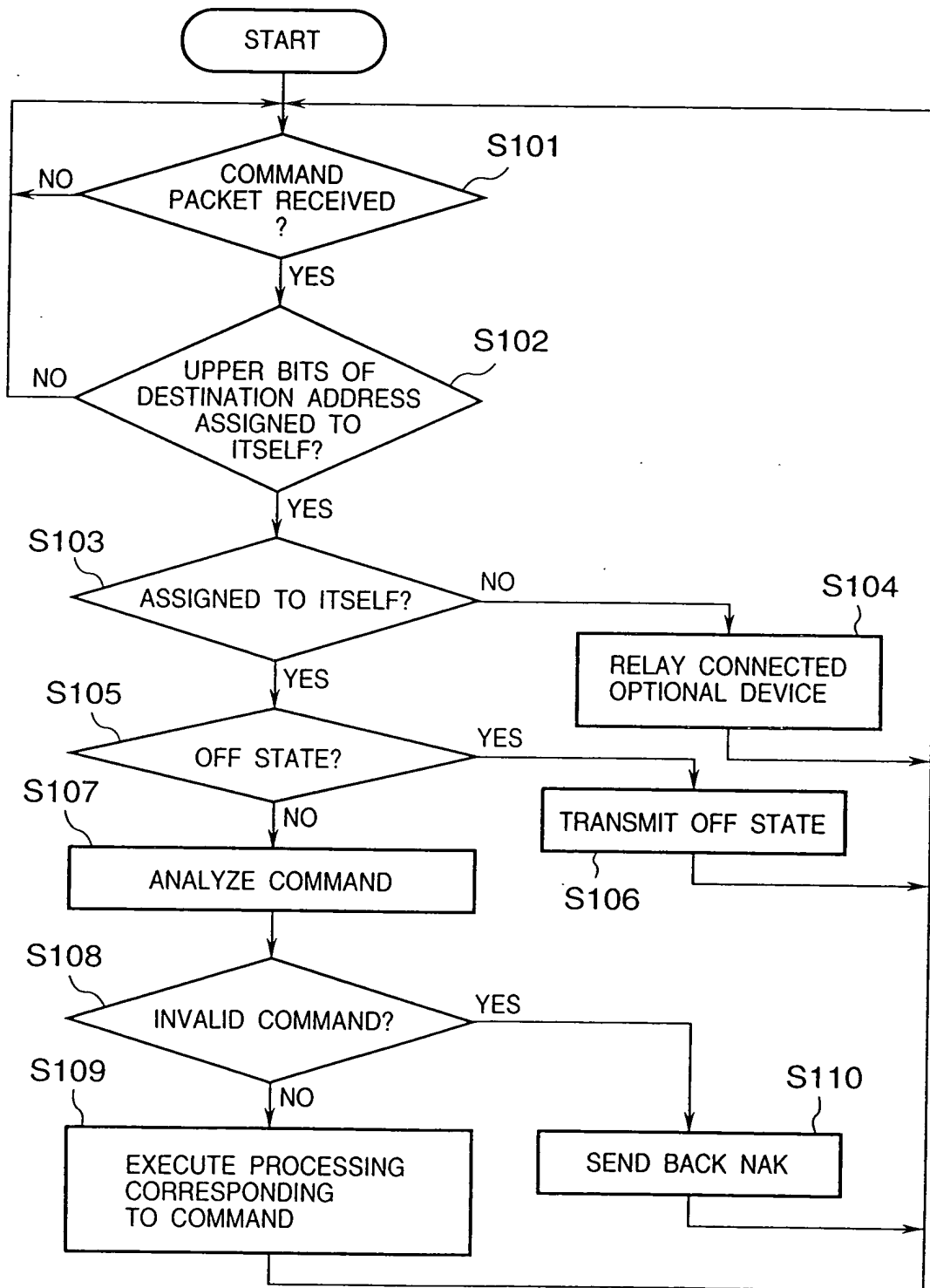
FIG. 38

FIG. 39

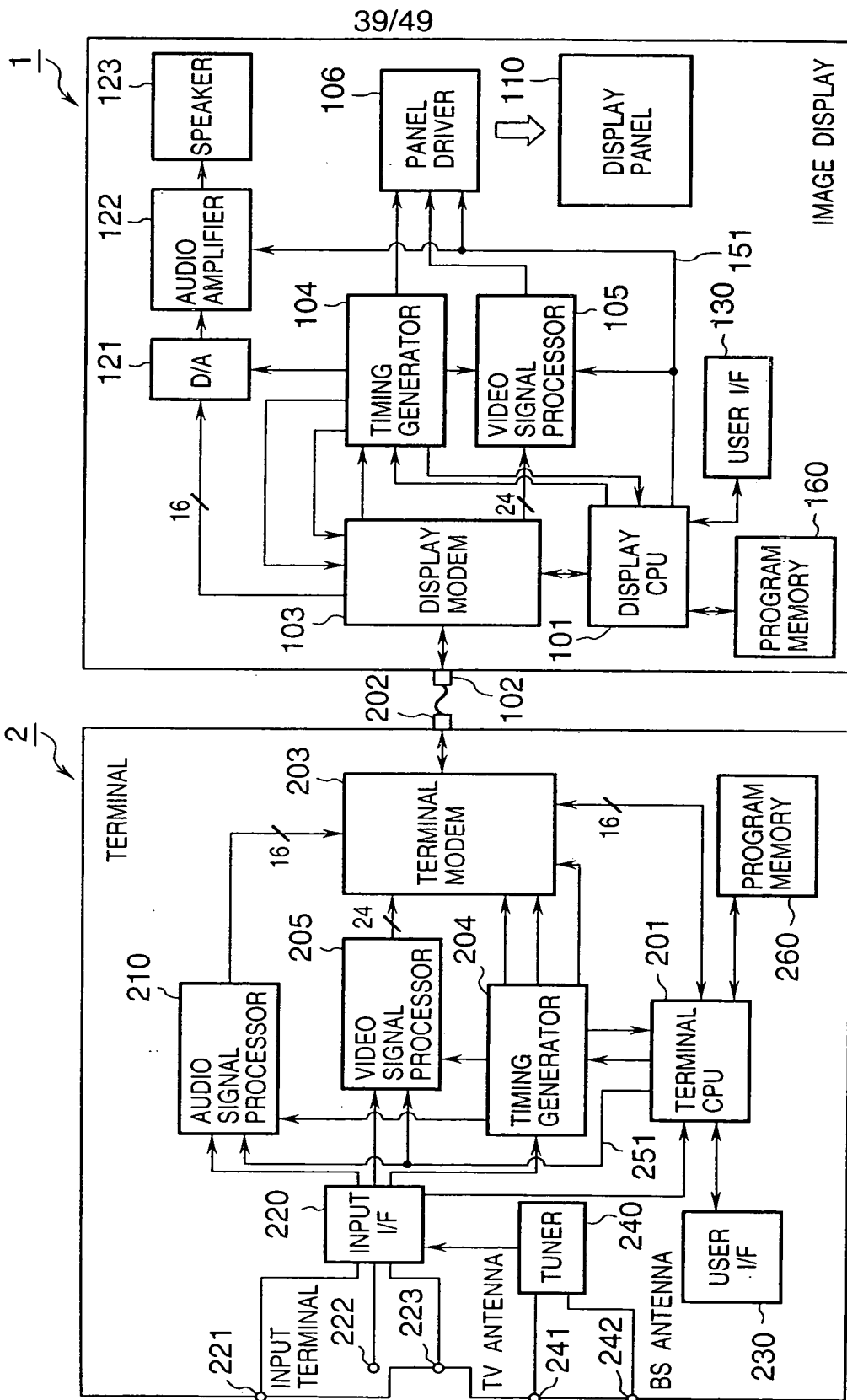


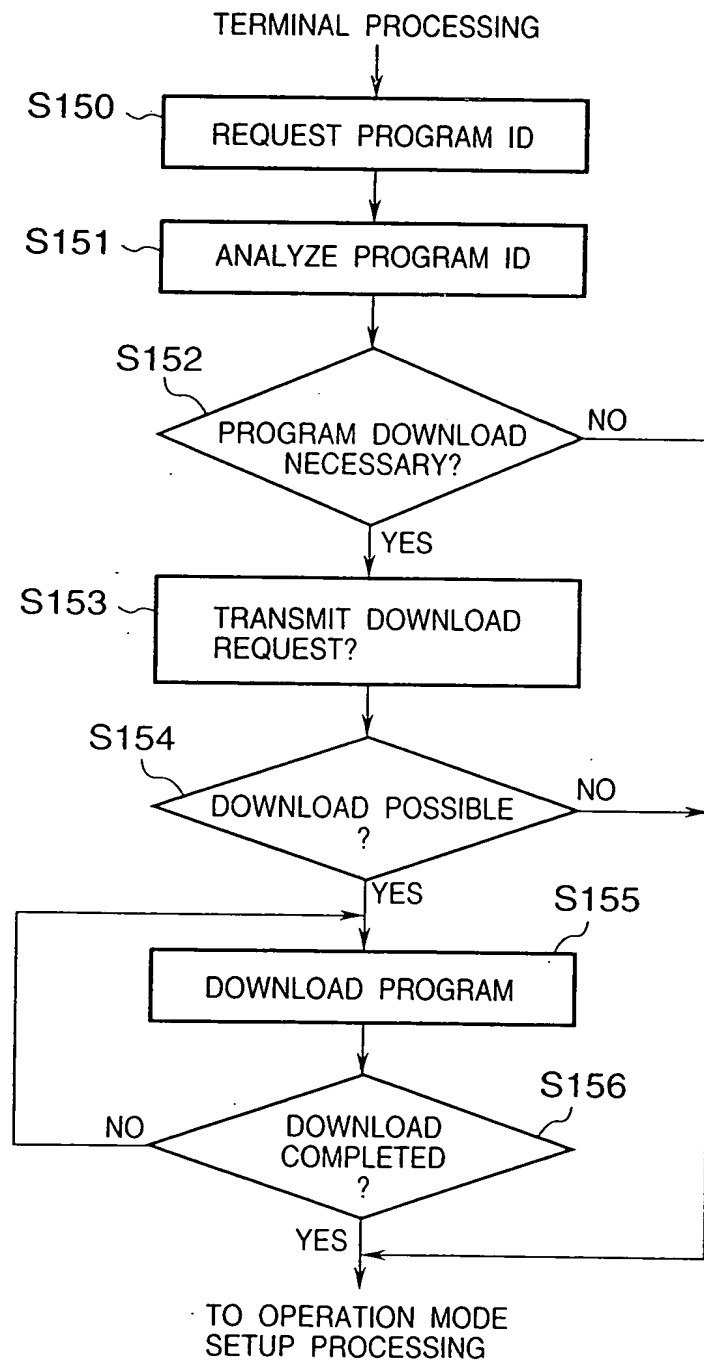
FIG. 40

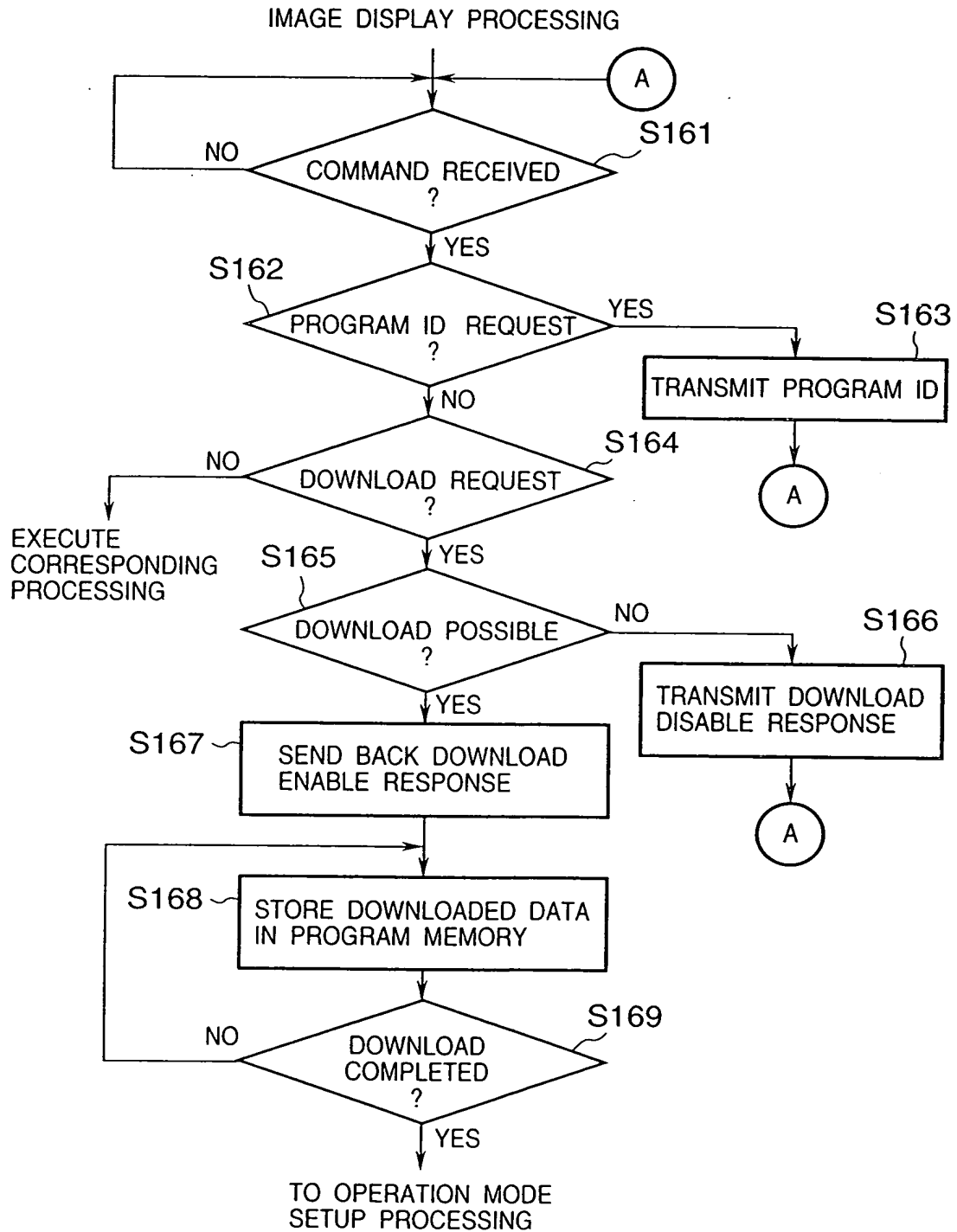
FIG. 41

FIG. 42

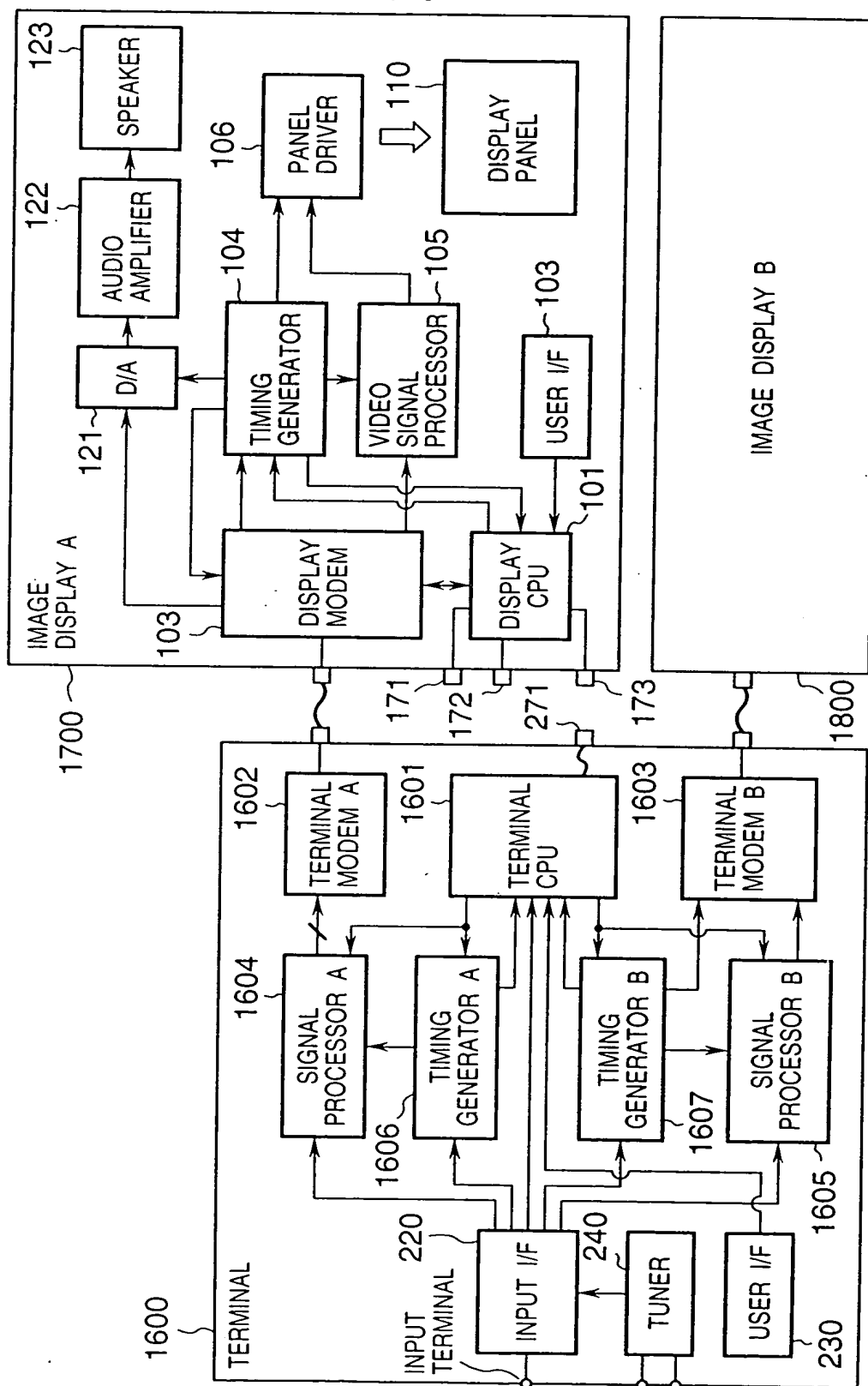


FIG. 43

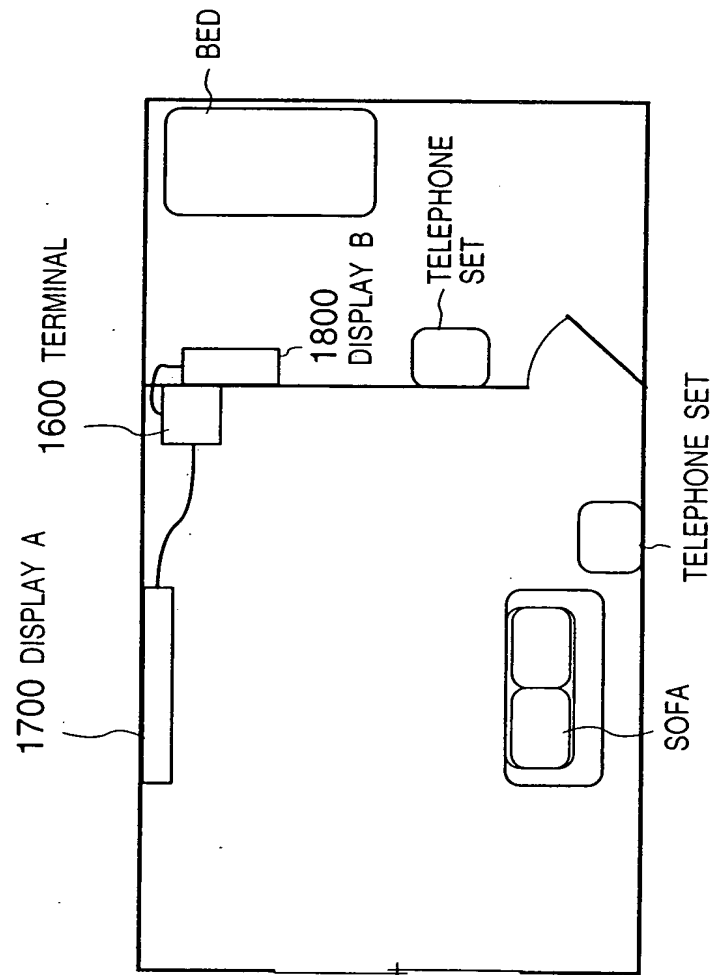


FIG. 44

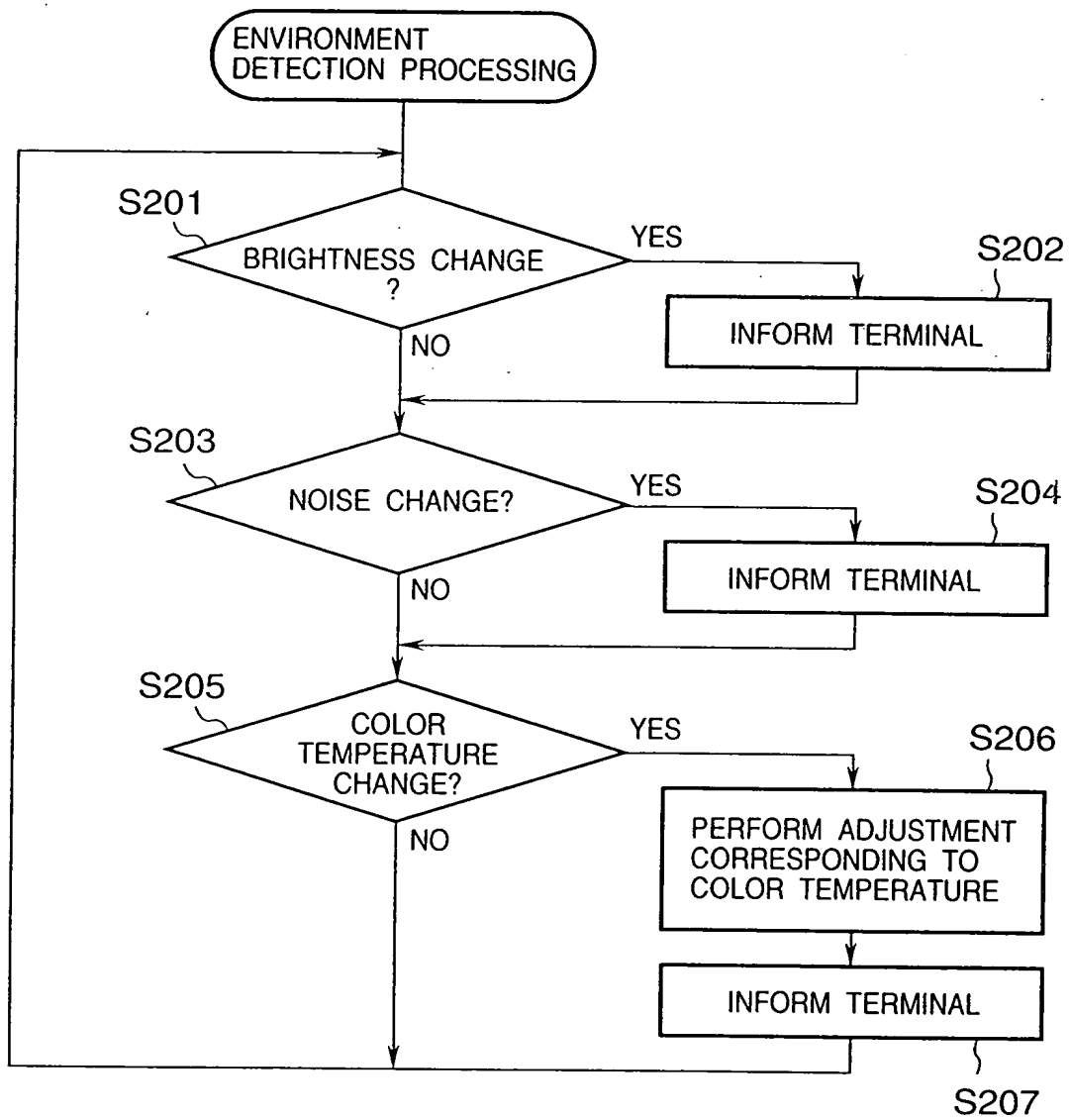


FIG. 45

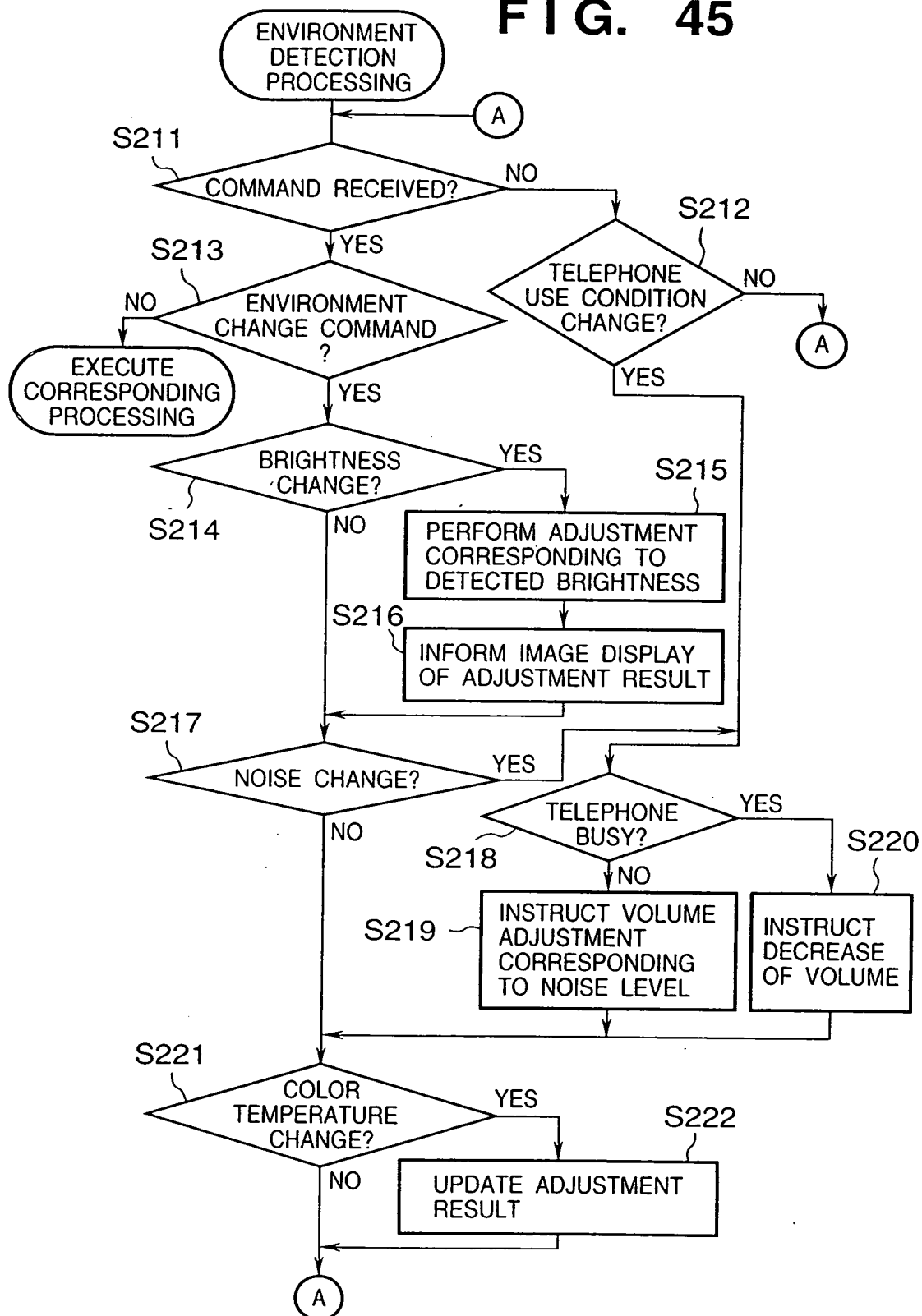


FIG. 46

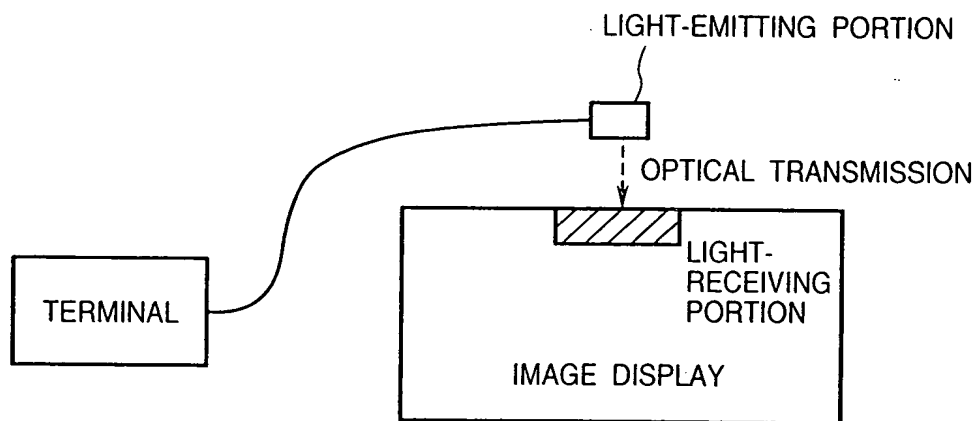


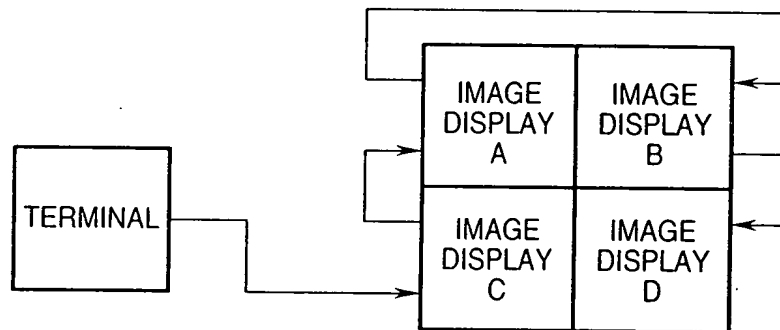
FIG. 47

FIG. 48

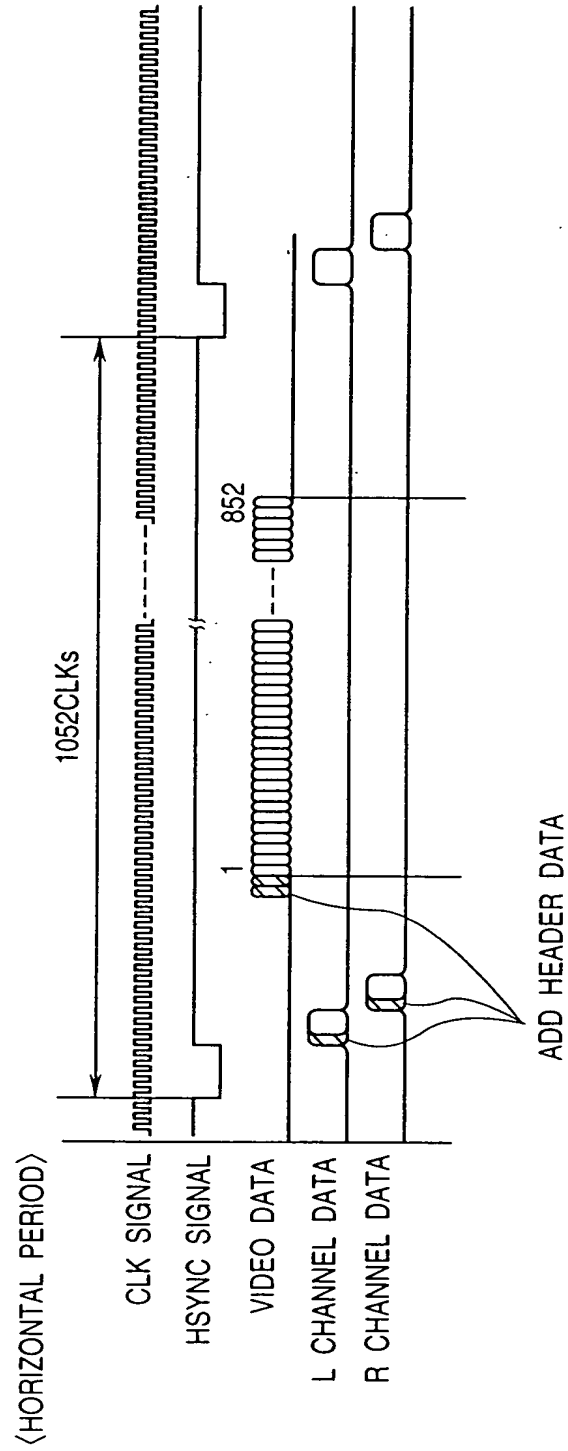


FIG. 49

PRIOR ART

